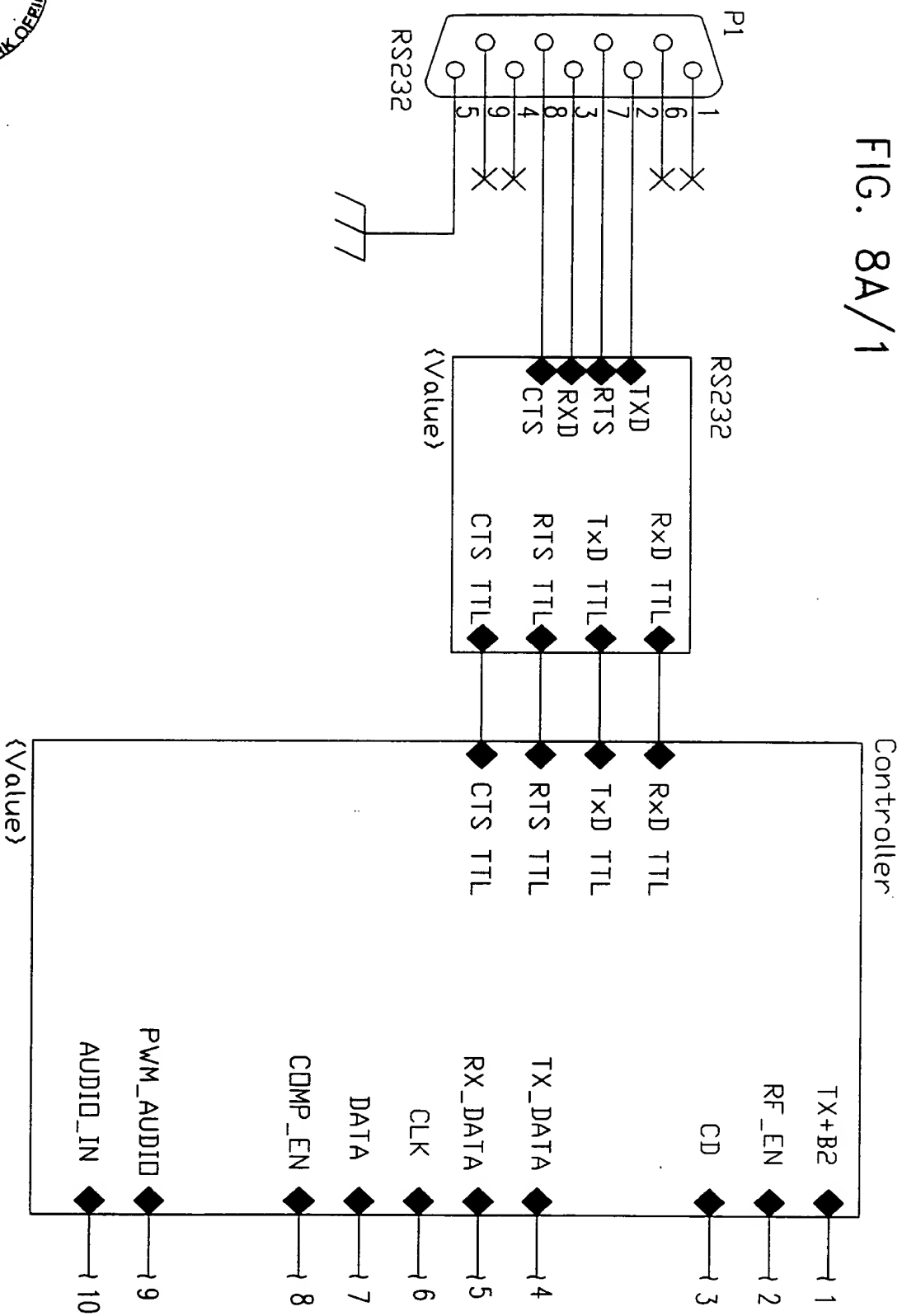


FIG. 8A/1



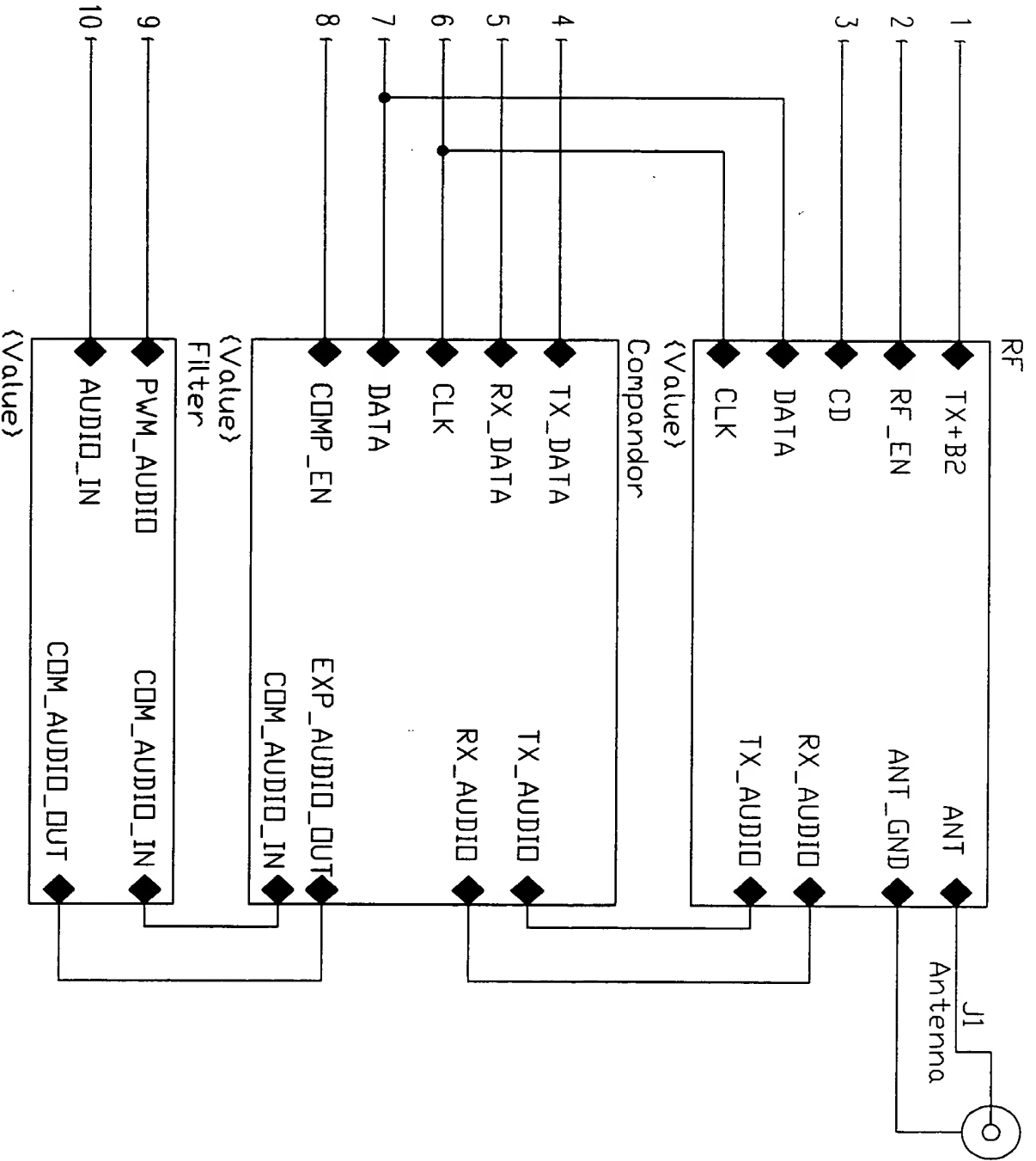


FIG. 8A/2

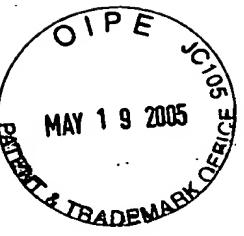
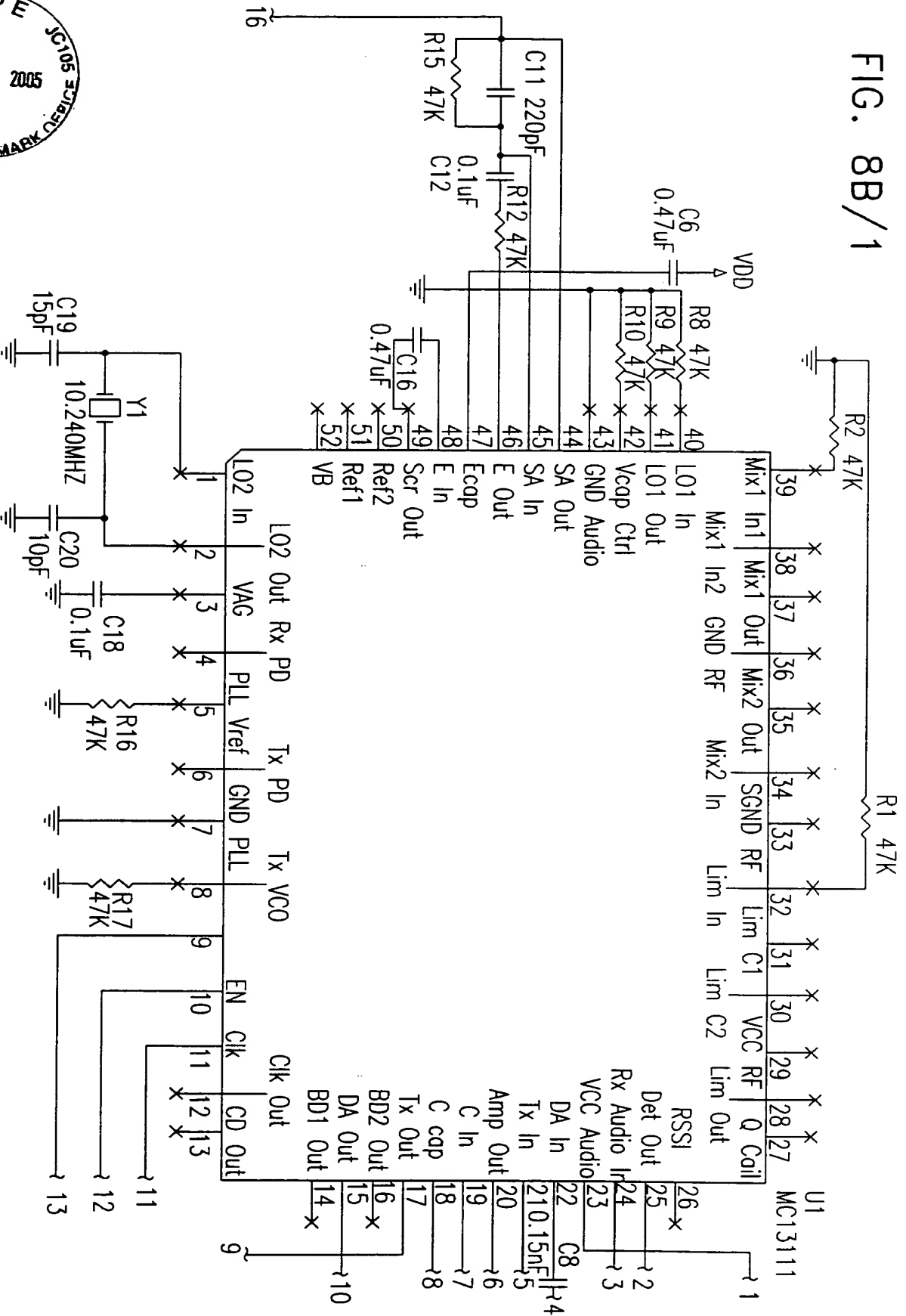
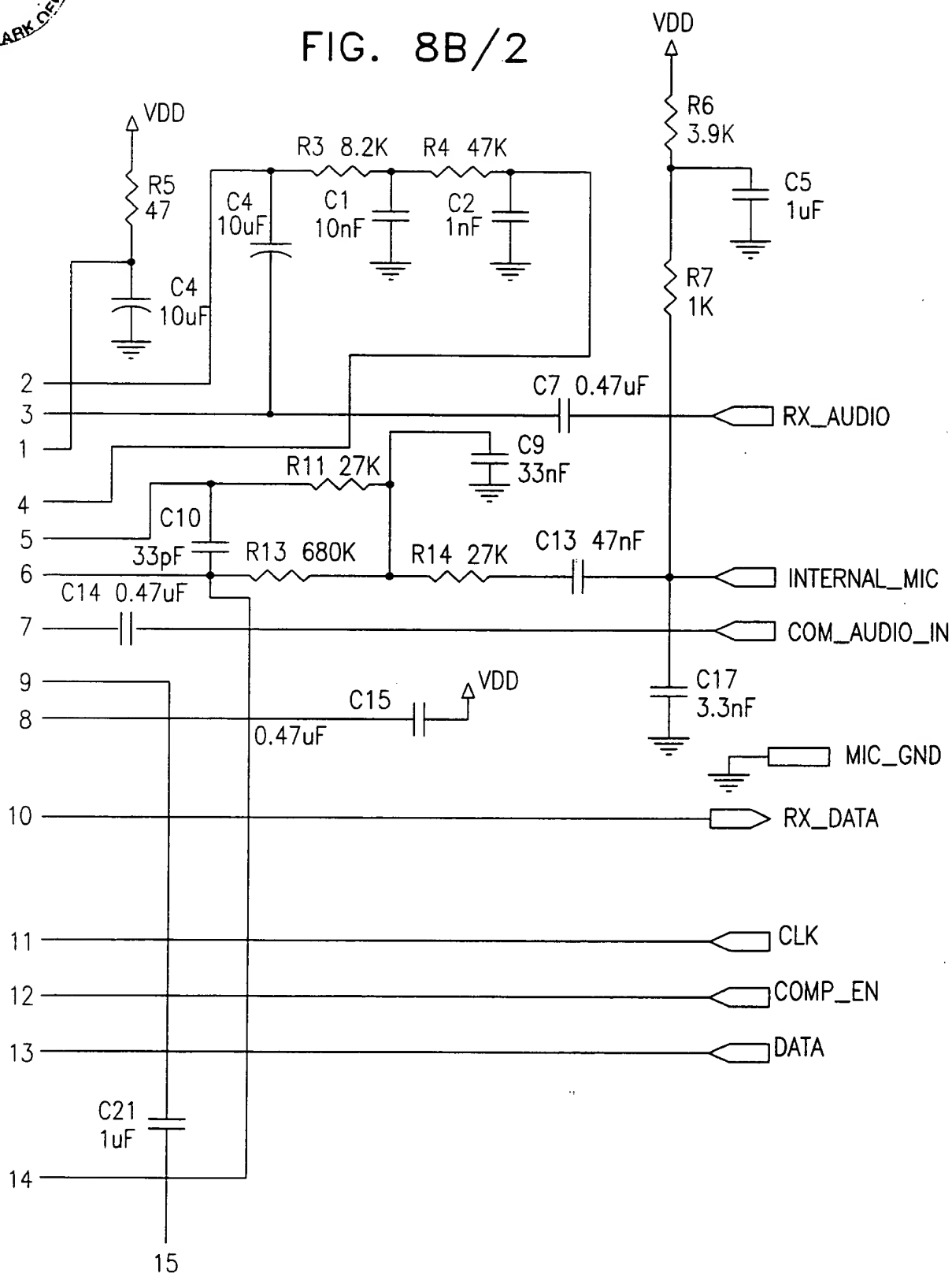


FIG. 8B/1





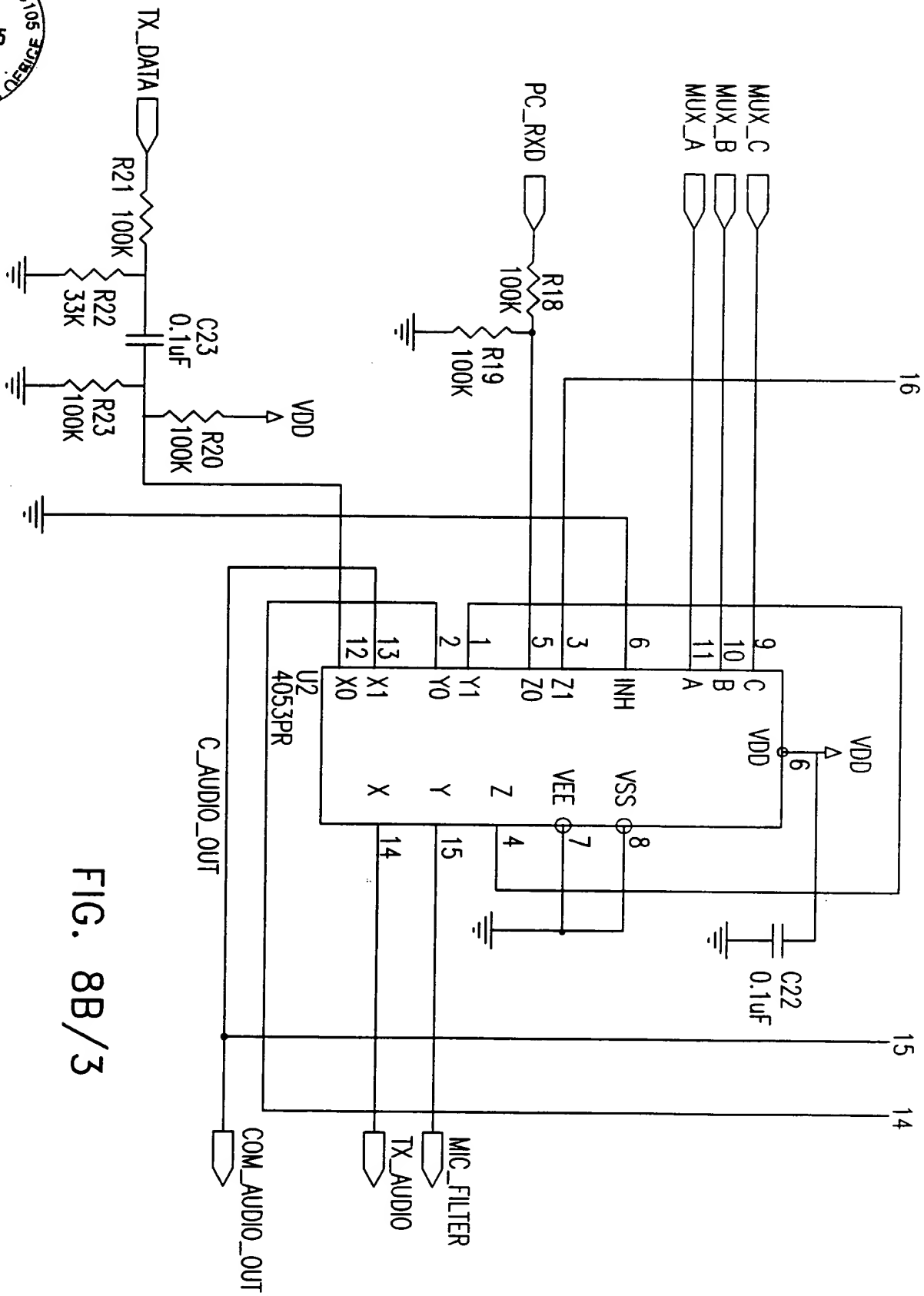
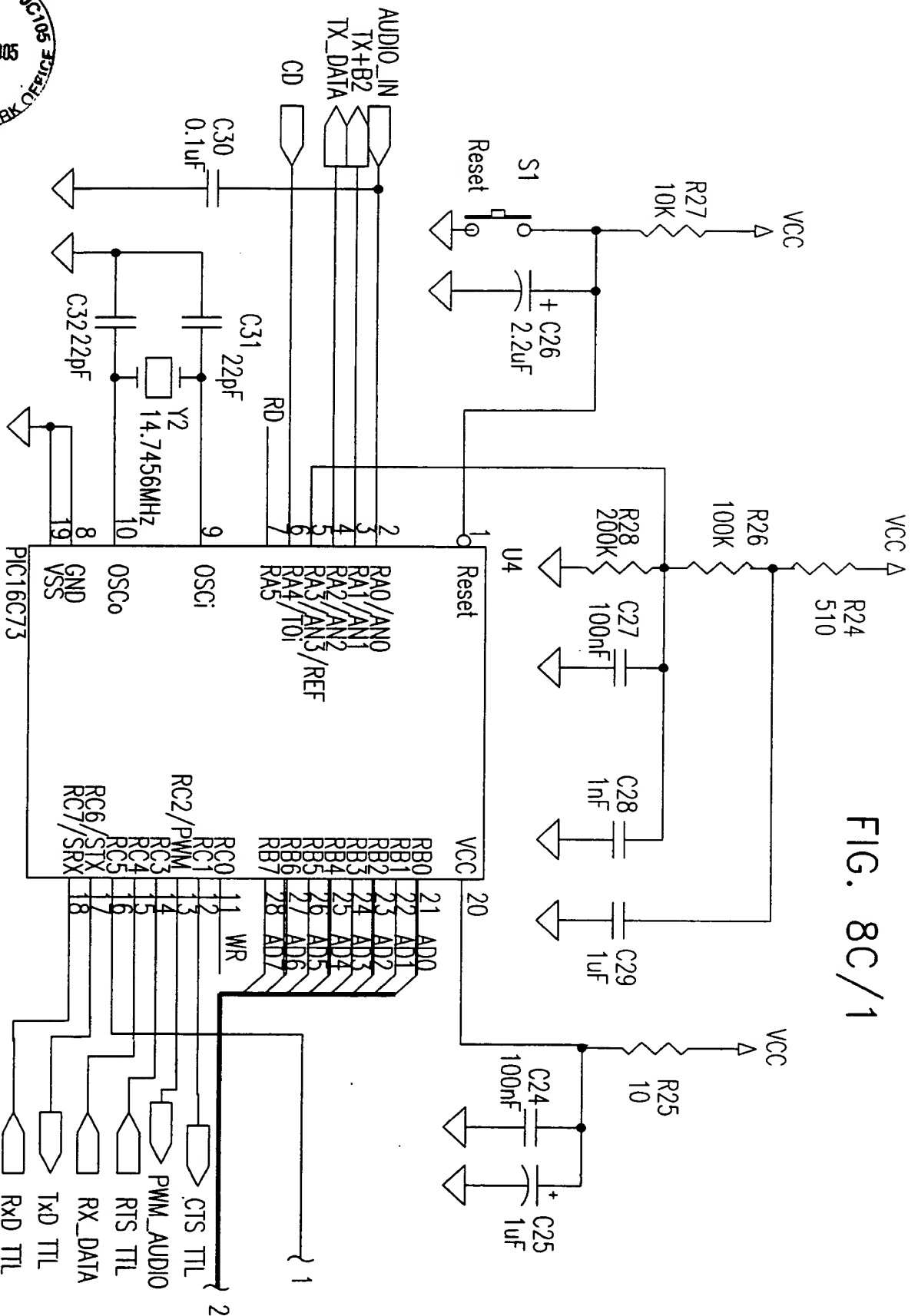


FIG. 8B/3



FIG. 8C/1



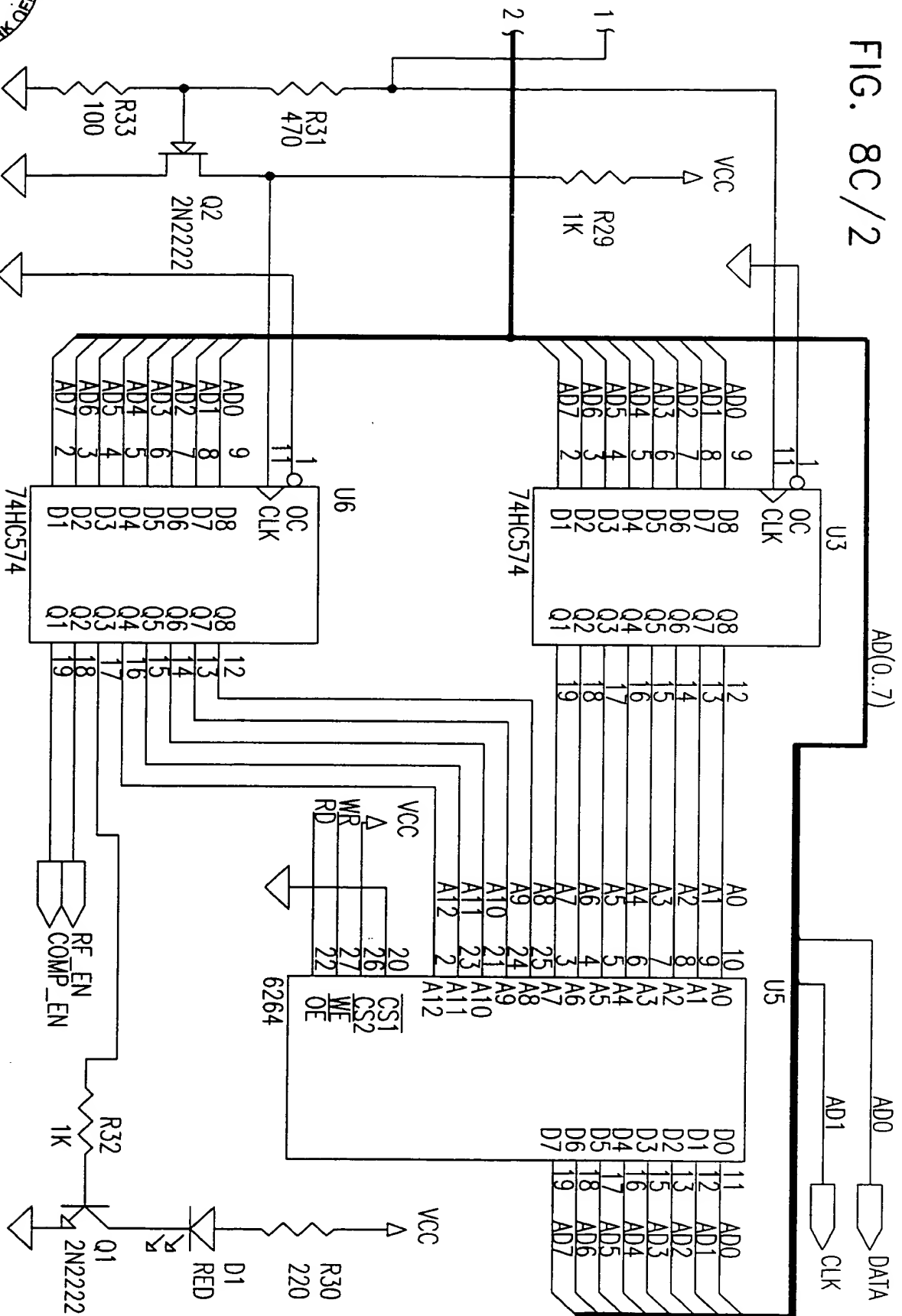
AD(0..7)

FIG. 8D/1

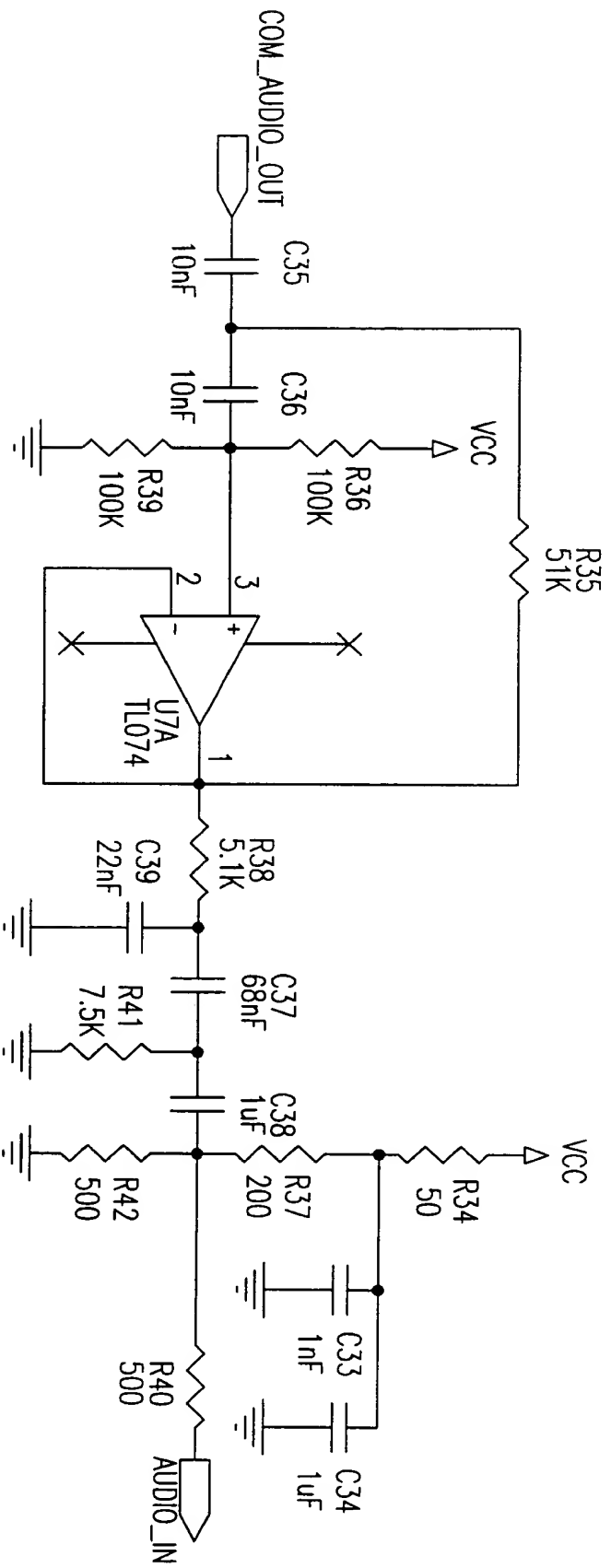


FIG. 8D/2

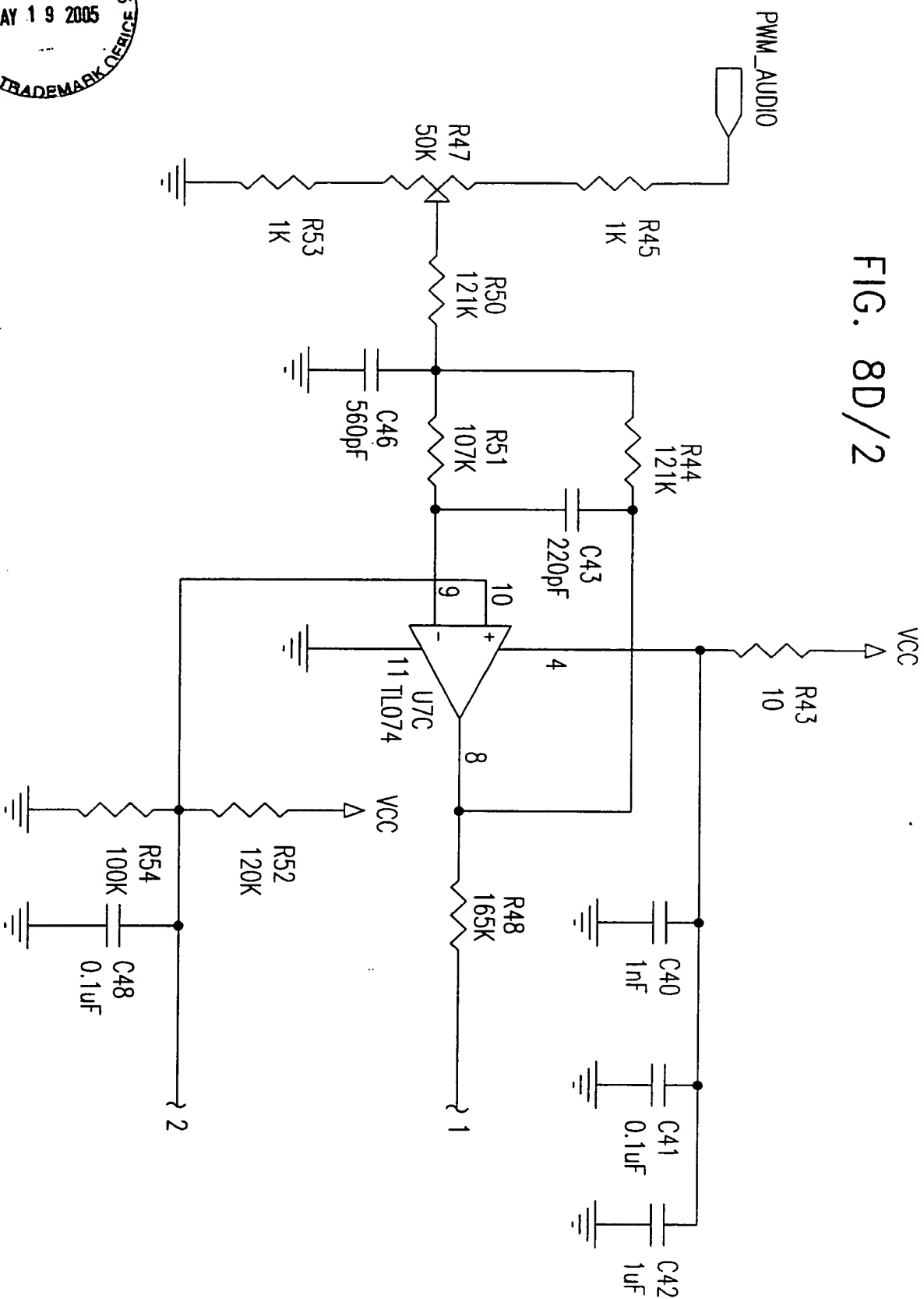


FIG. 8D/3

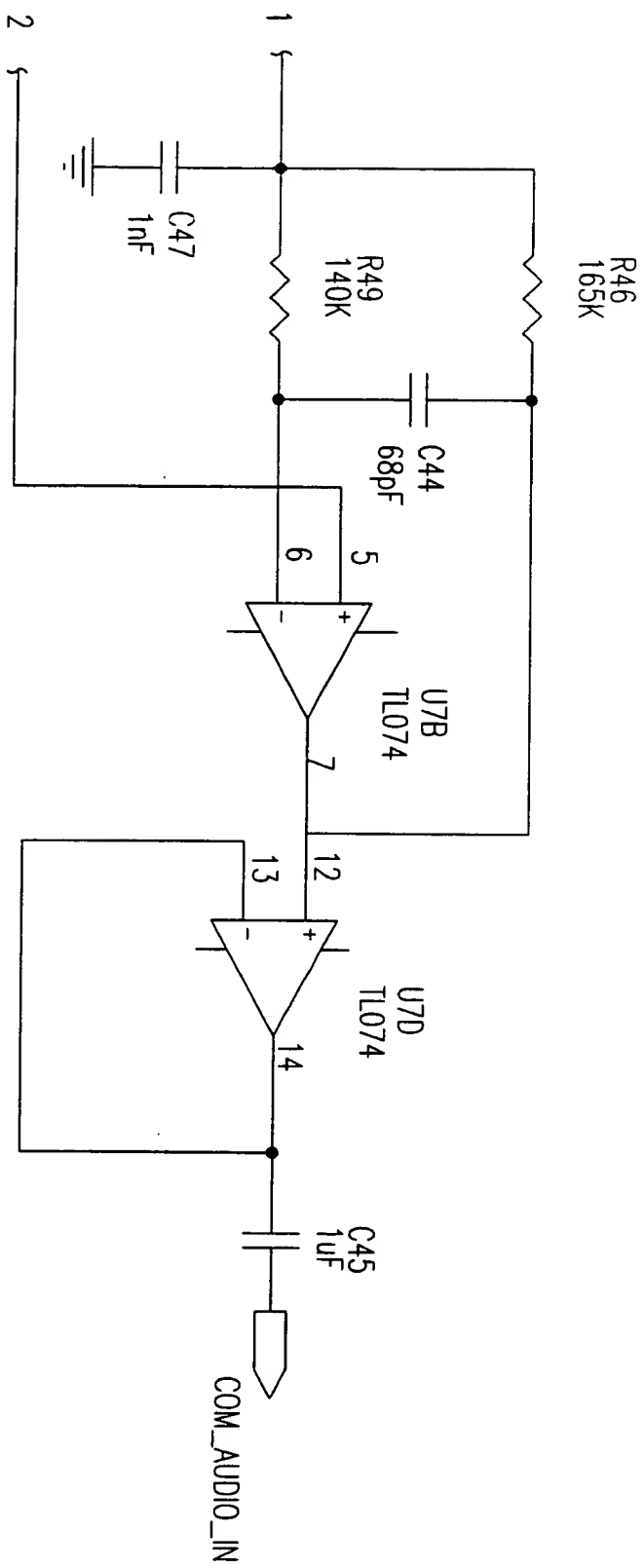


FIG. 8E

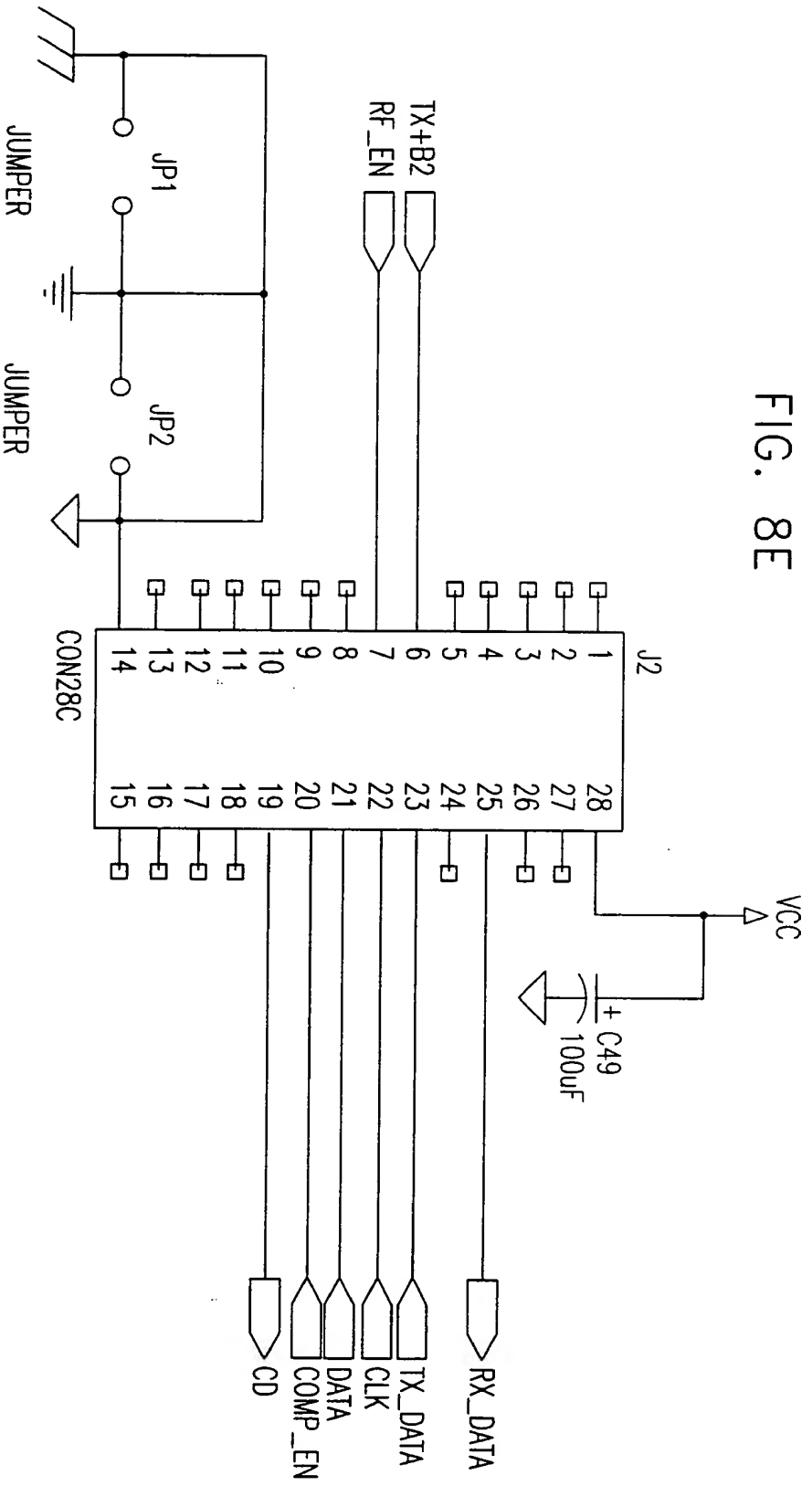


FIG. 8F

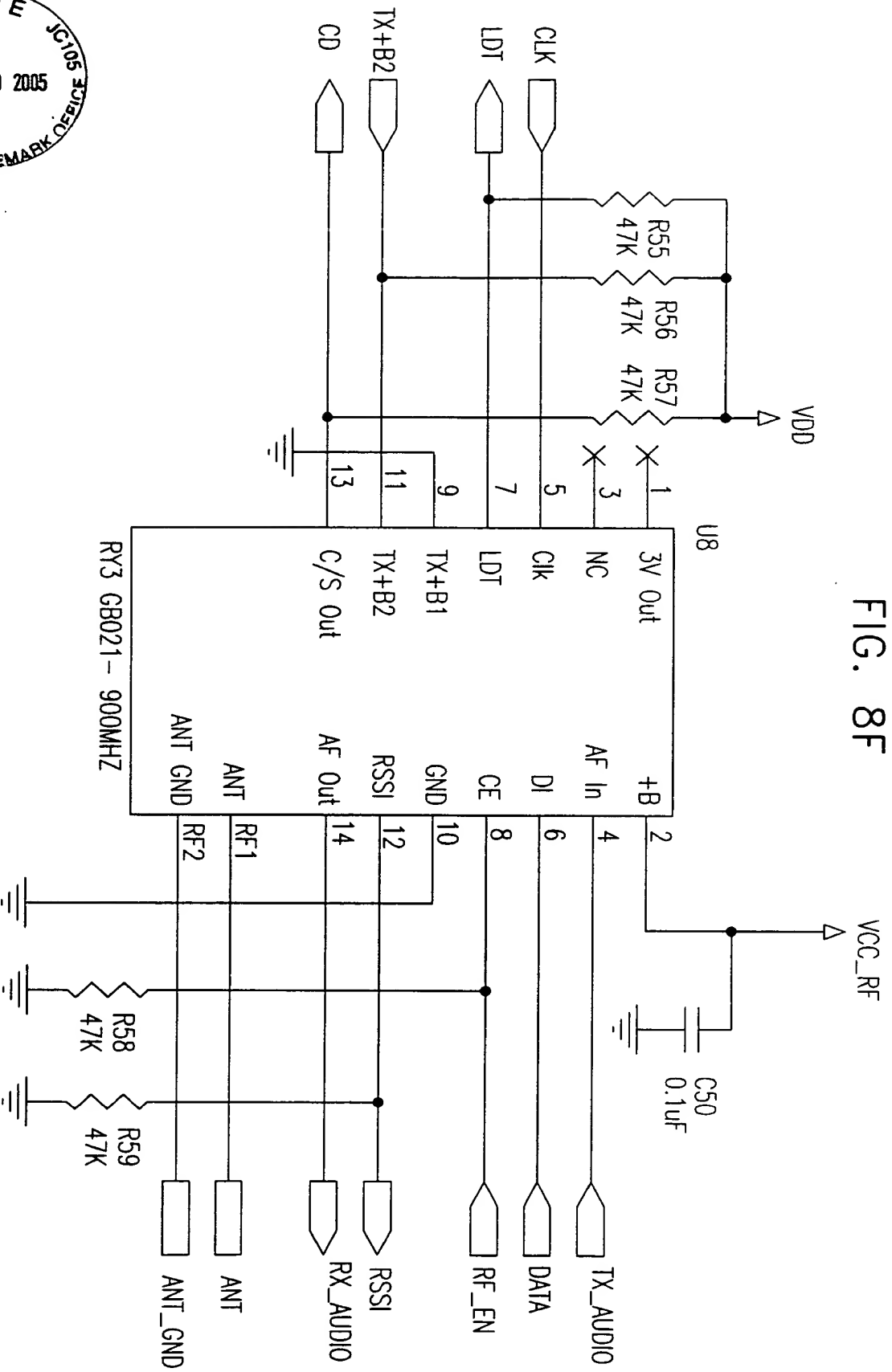


FIG. 8C/1

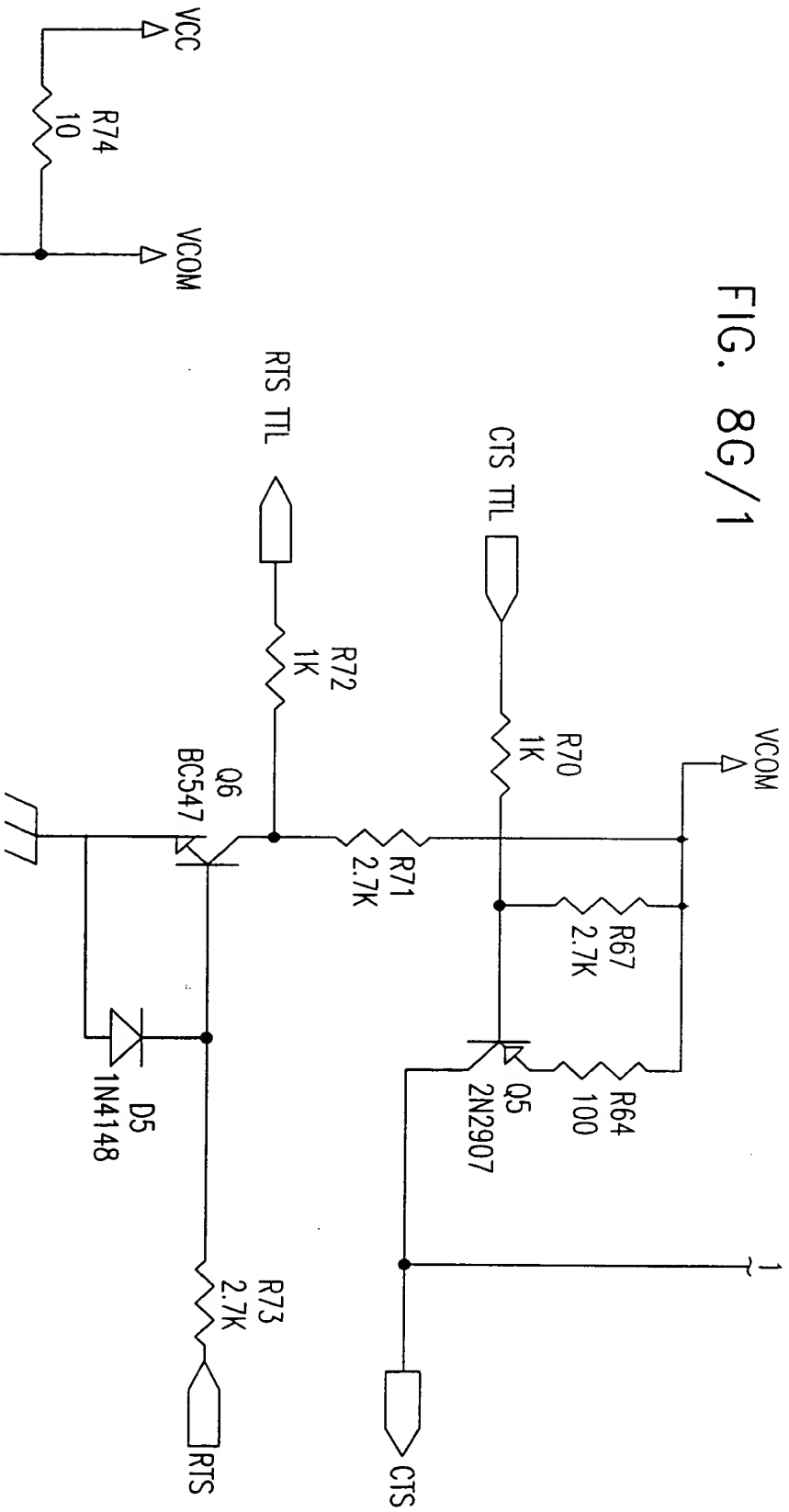
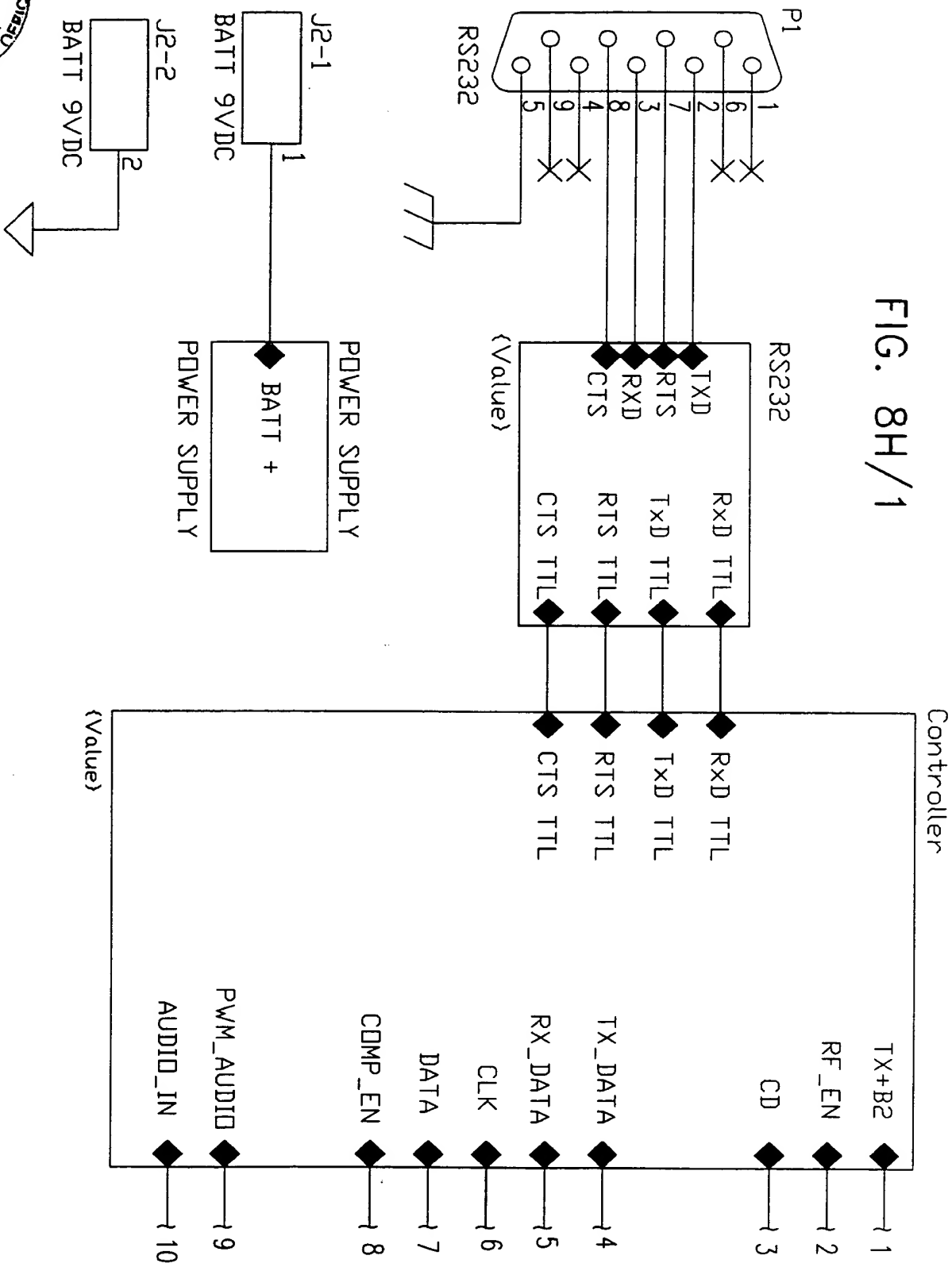




FIG. 8H/1



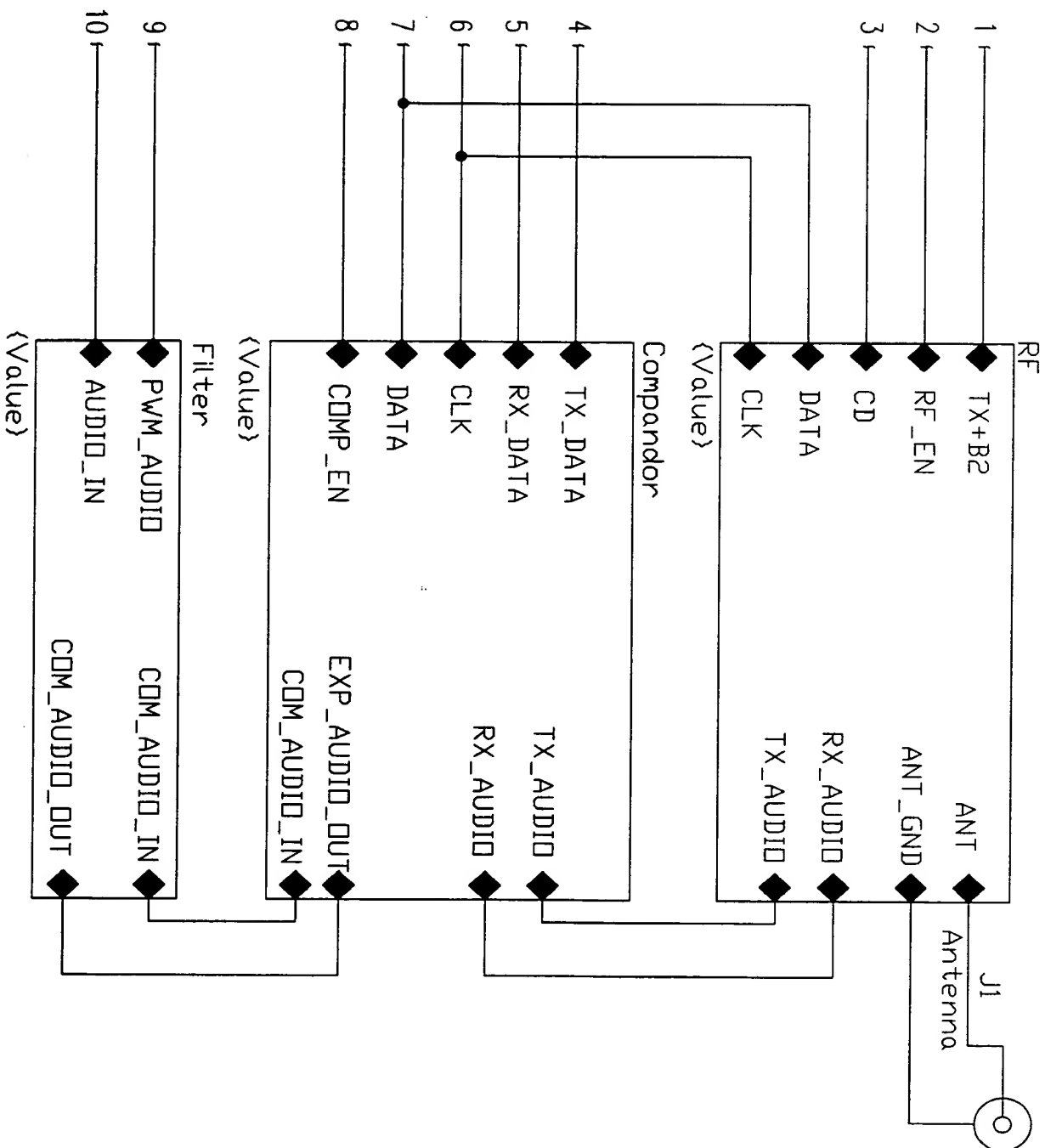


FIG. 8H/2

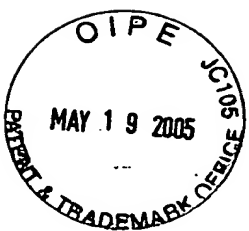
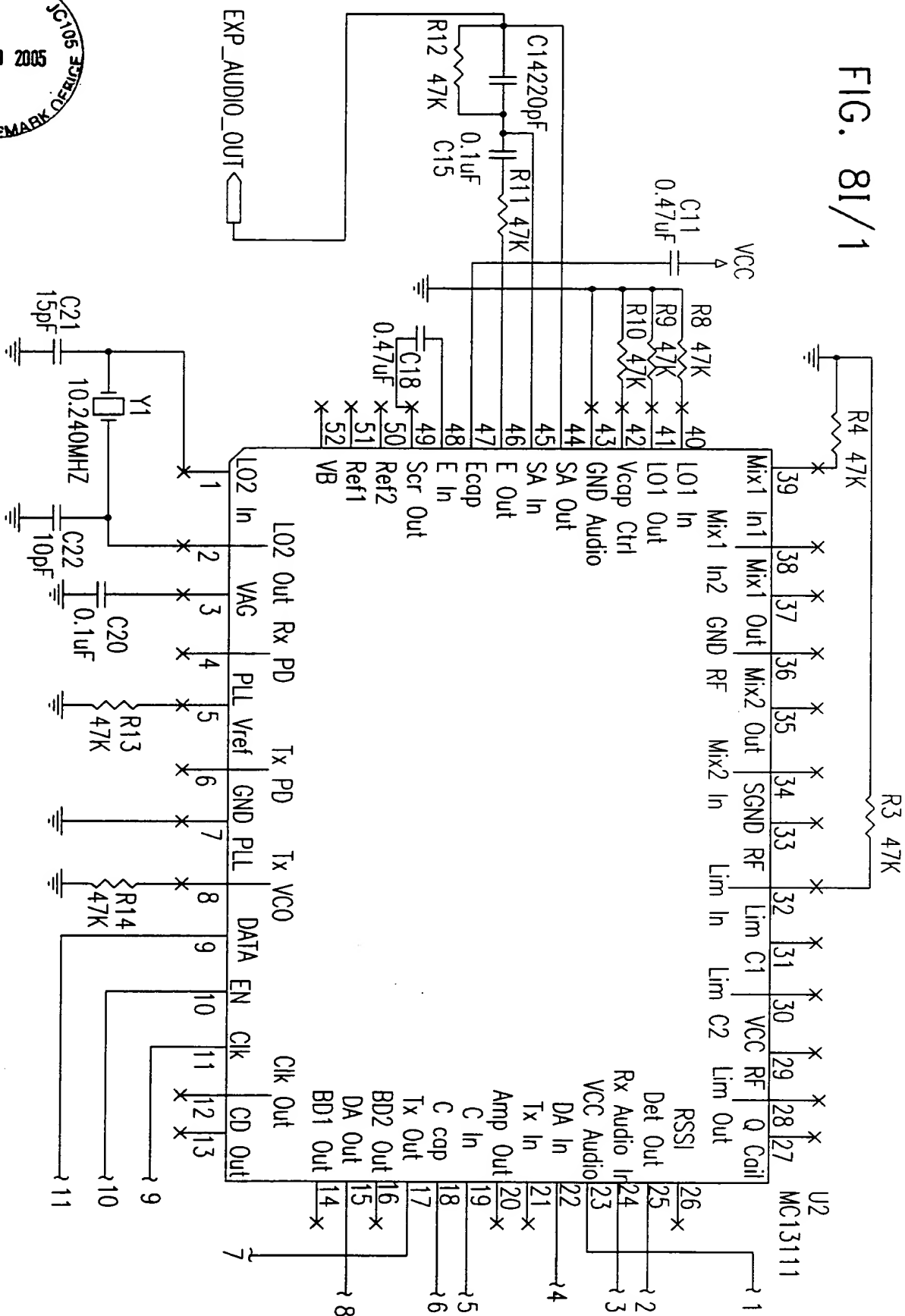


FIG. 81/1



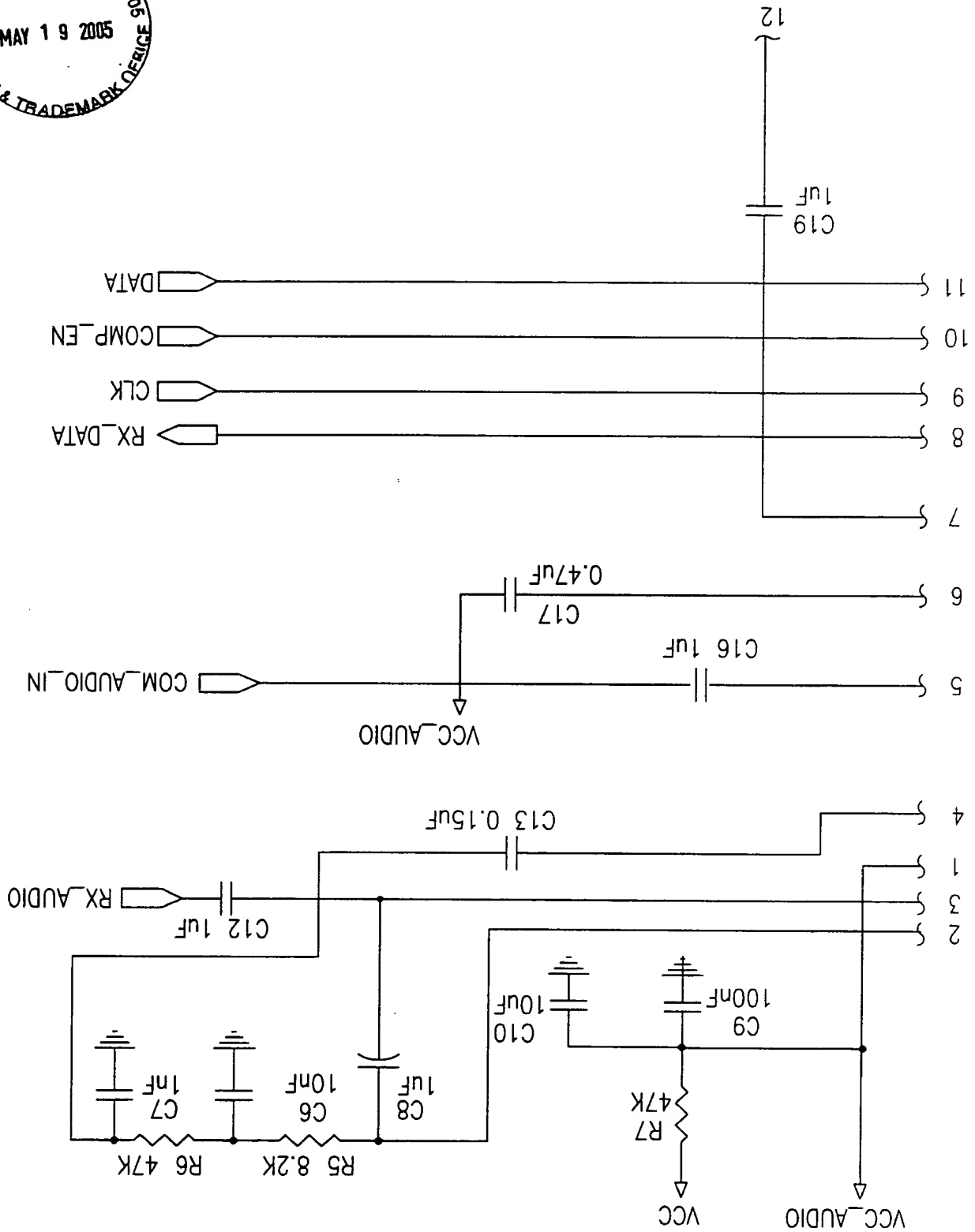


FIG. 81/2

09/602,892

FIG. 81/3

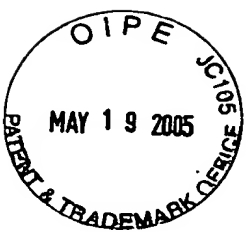
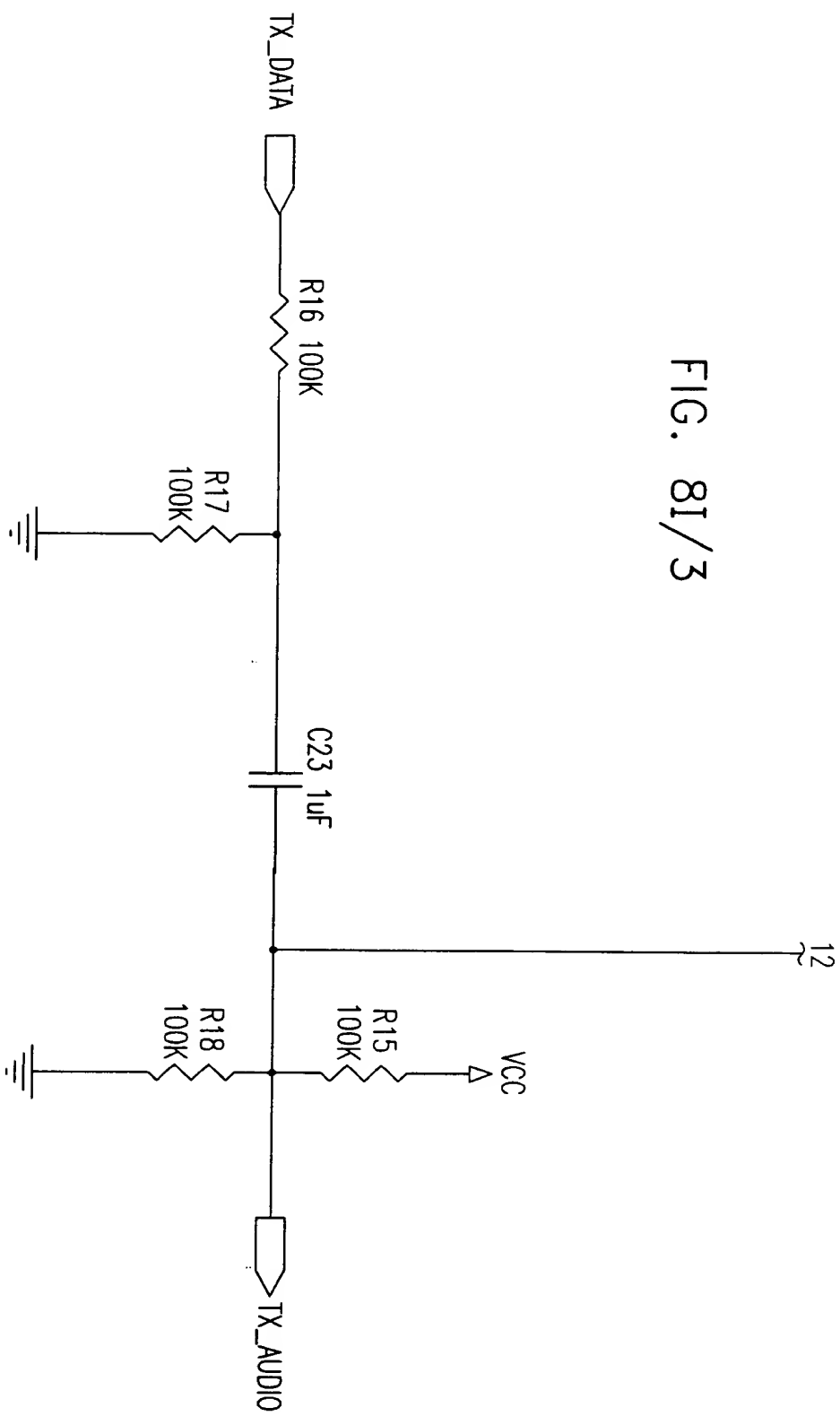


FIG. 8J/1

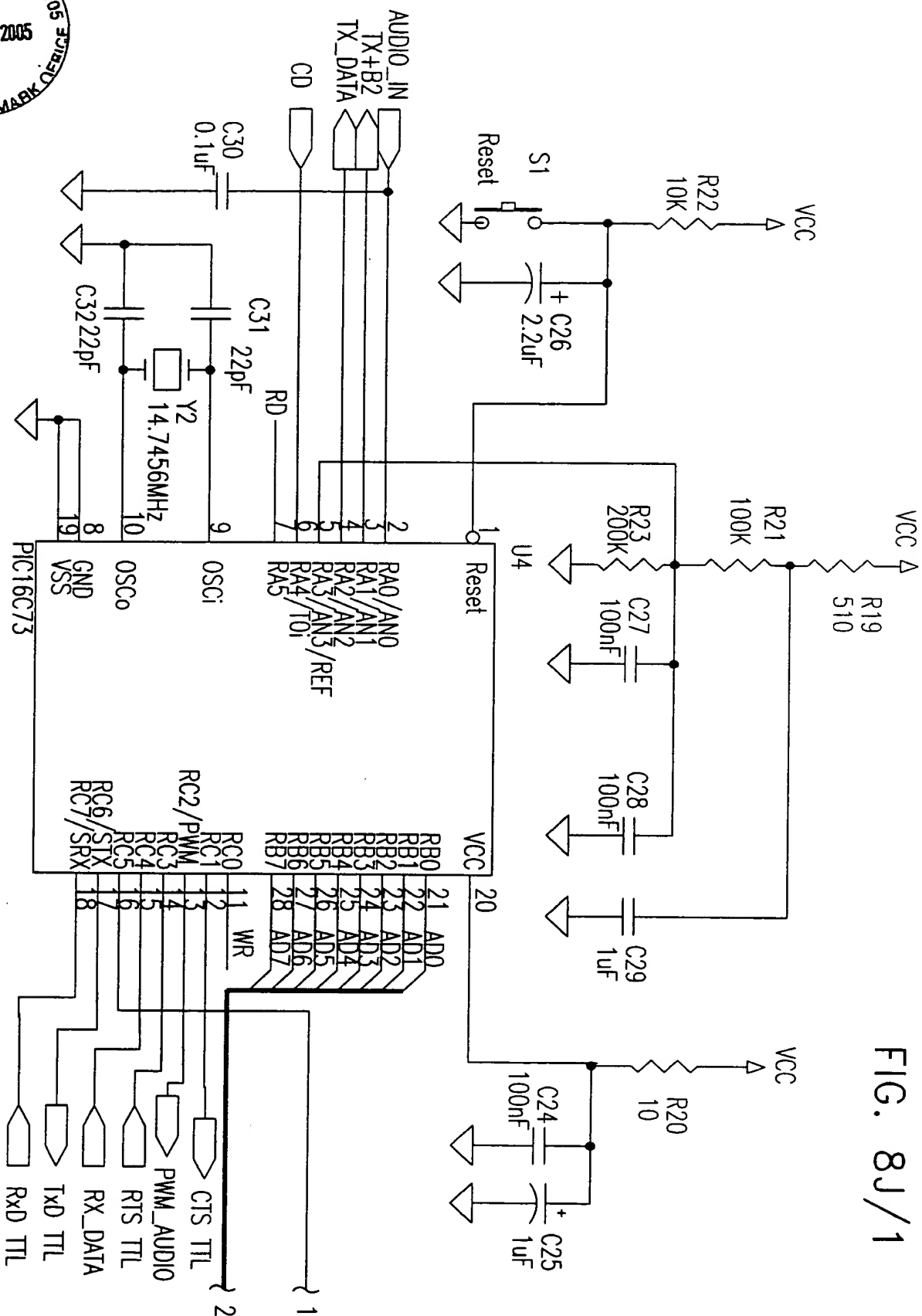


FIG. 8J/2

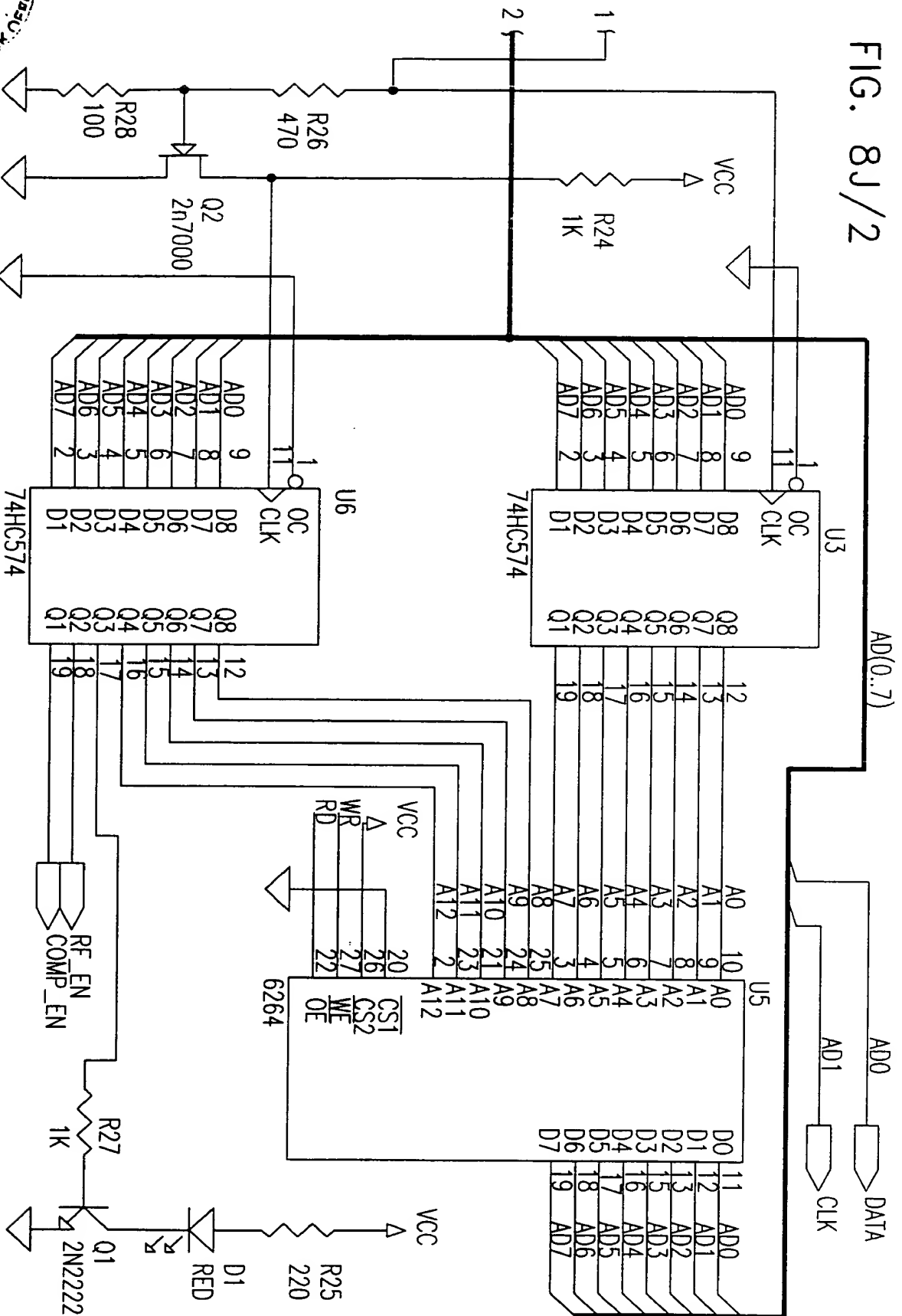


FIG. 8K/1

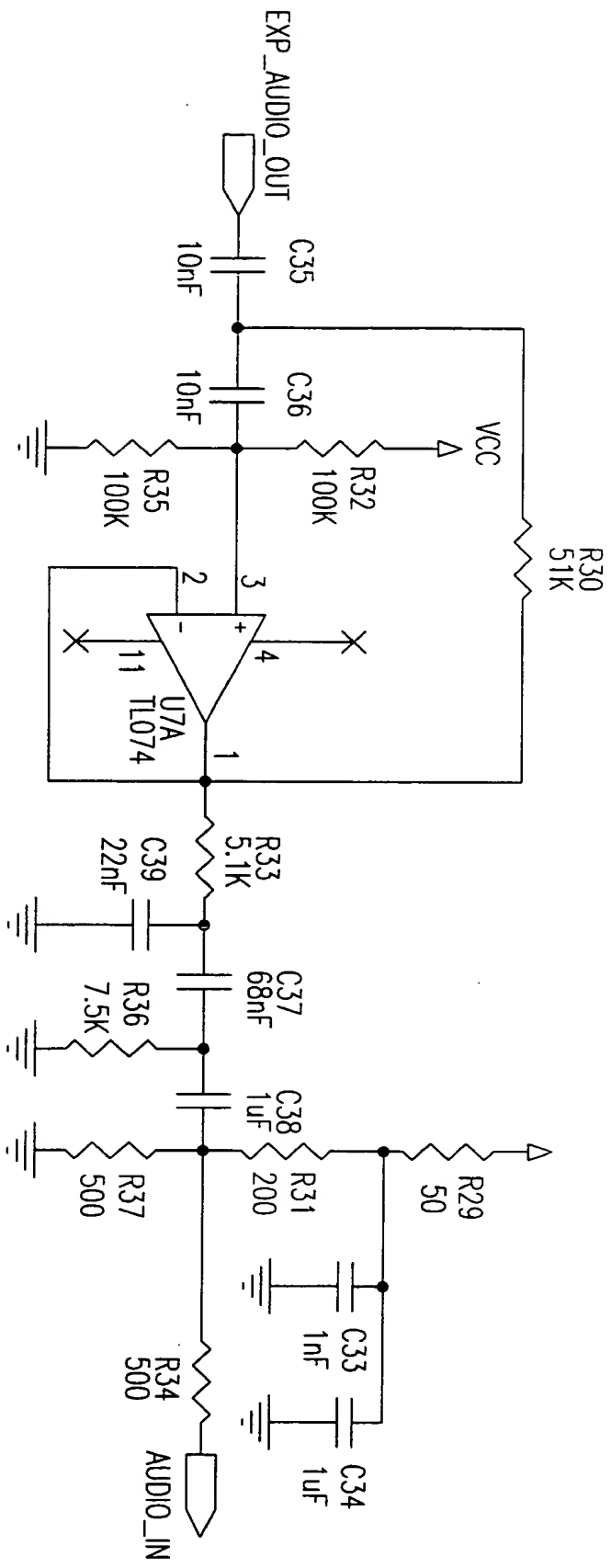


FIG. 8K/2

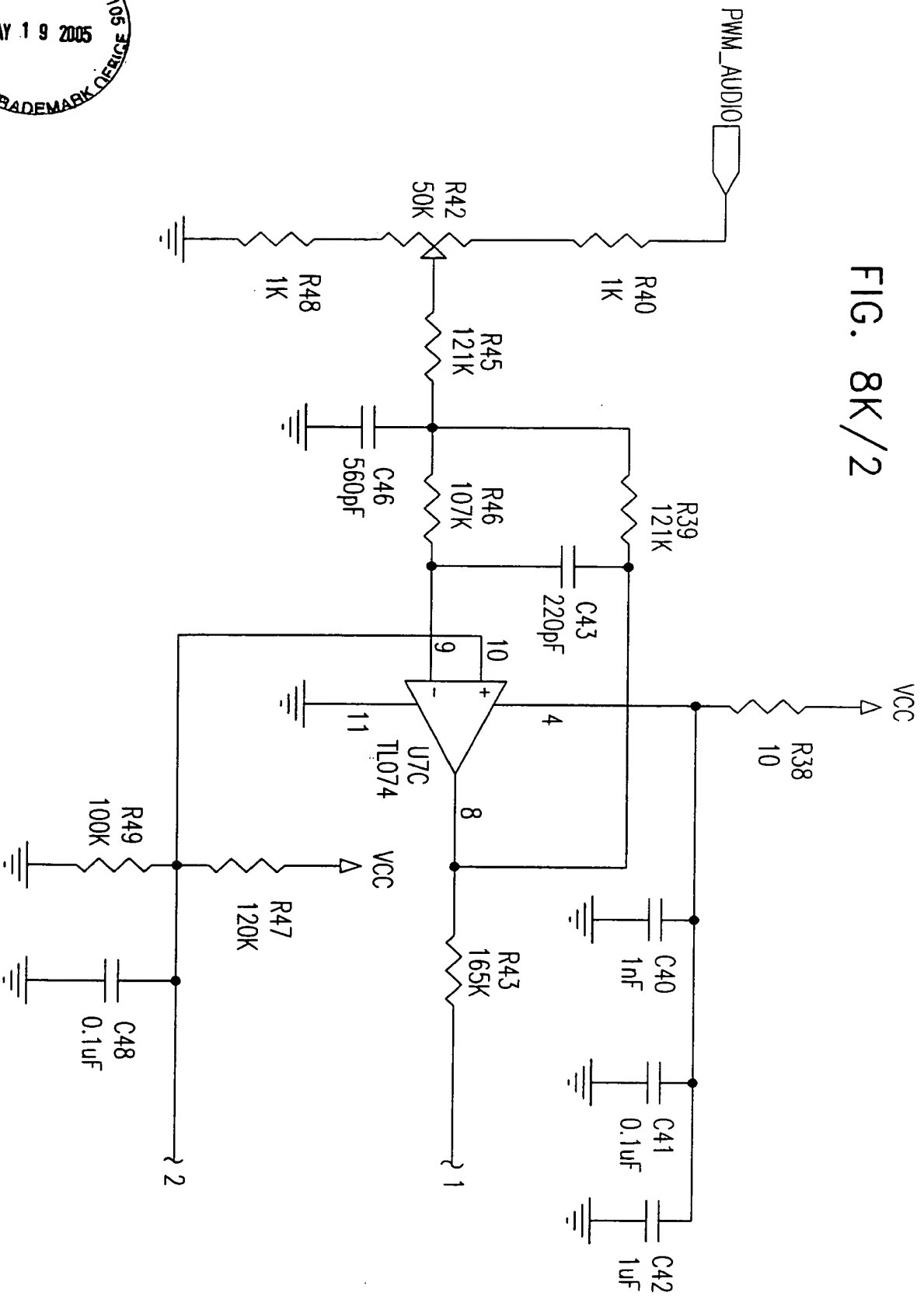


FIG. 8K/3

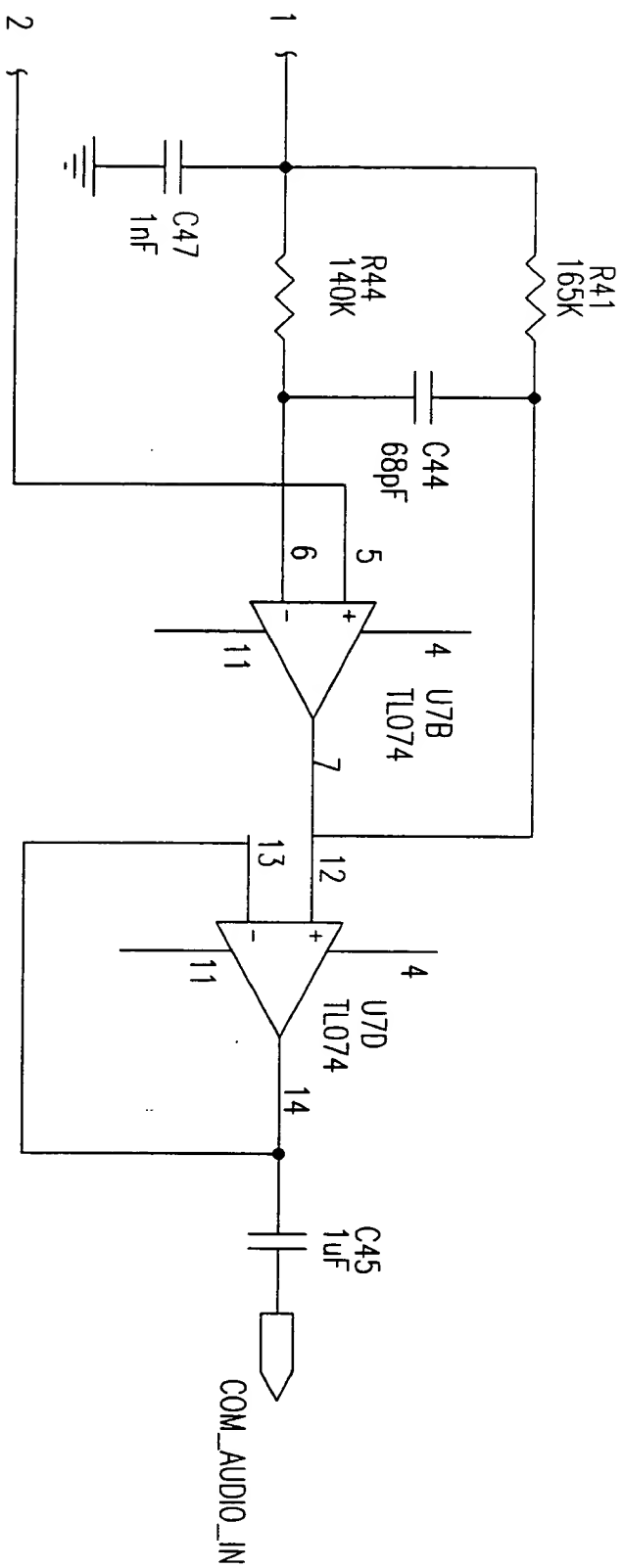


FIG. 8L

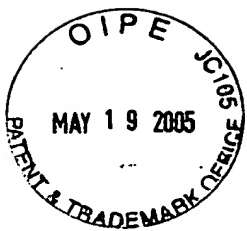
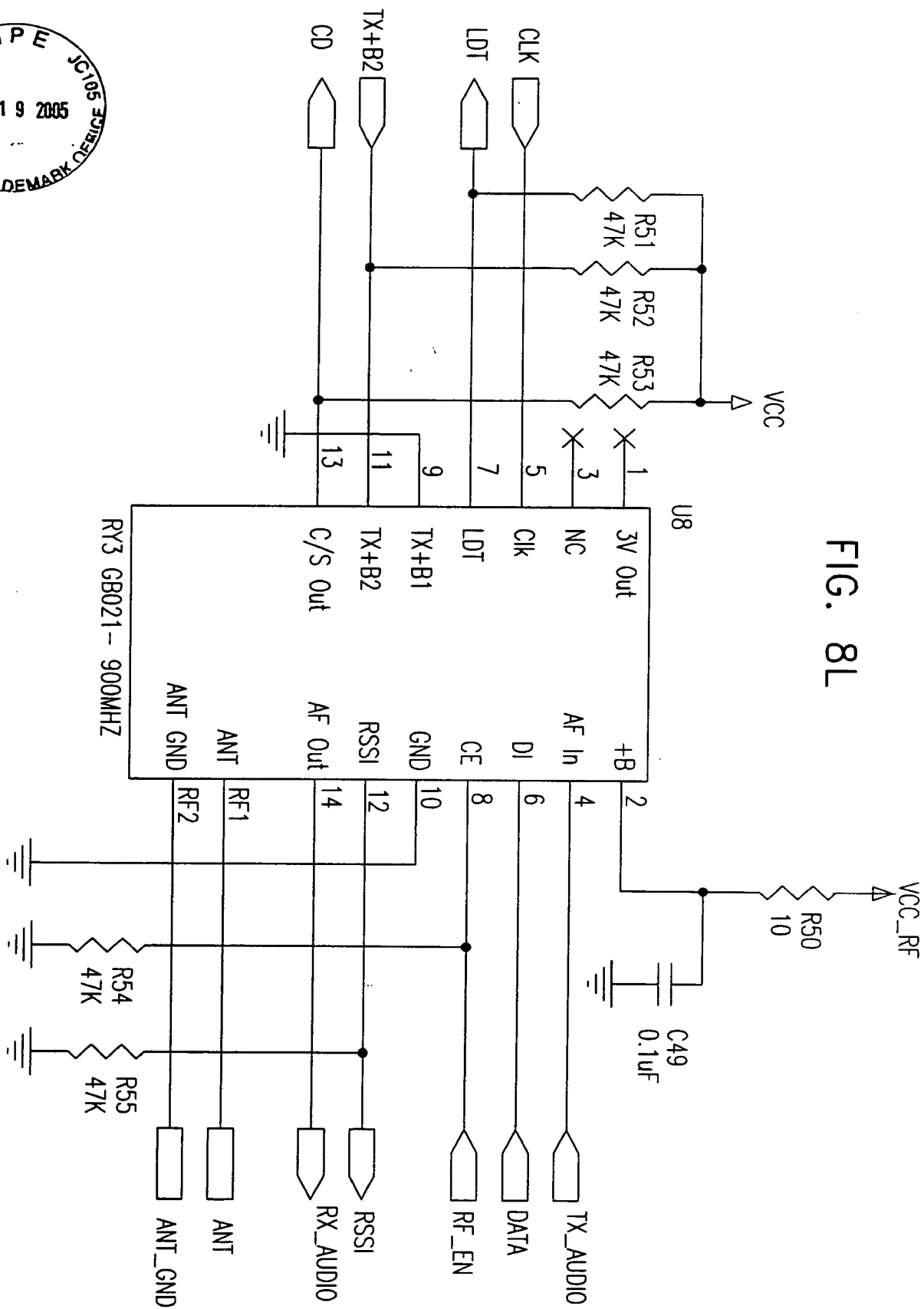


FIG. 8M

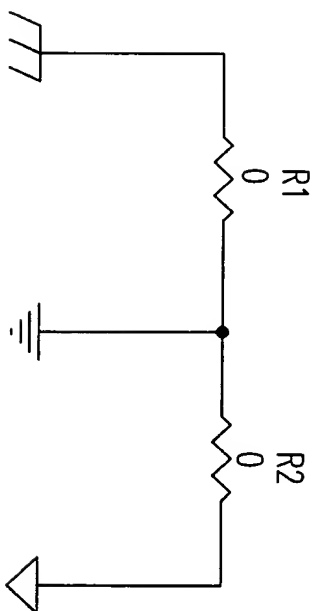
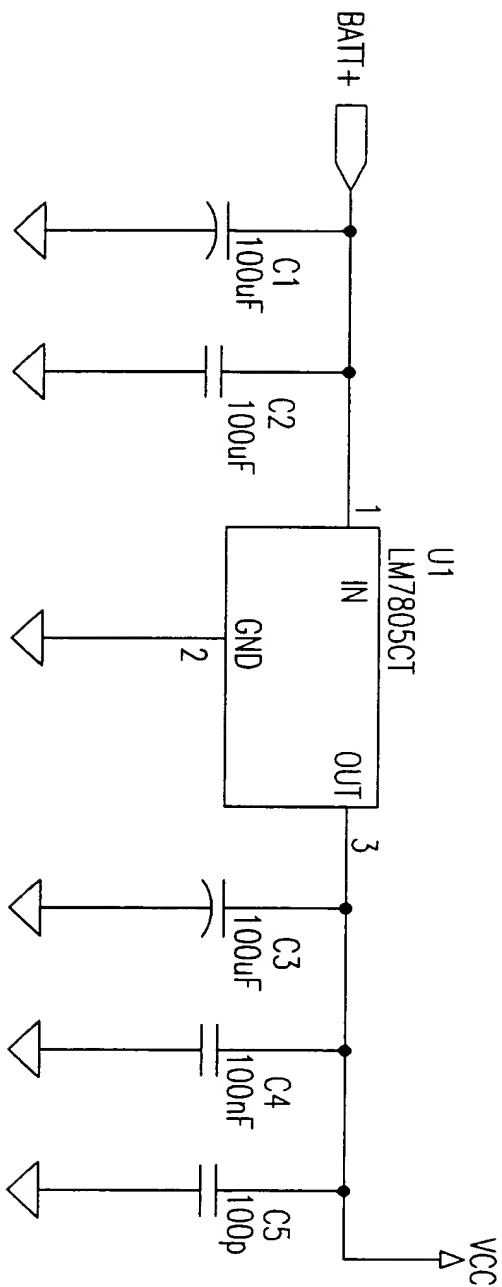


FIG. 8N/1

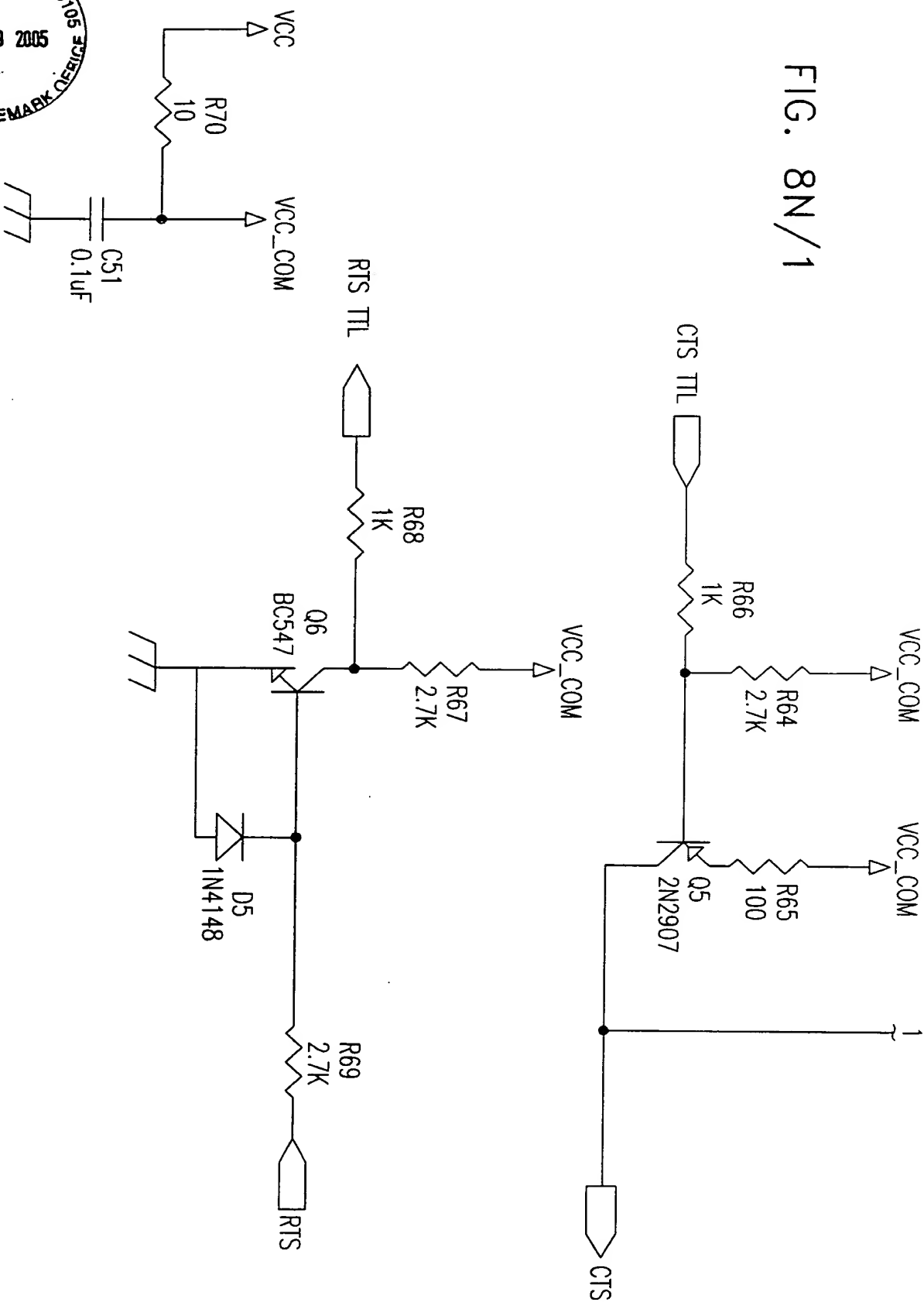


FIG. 8N/2

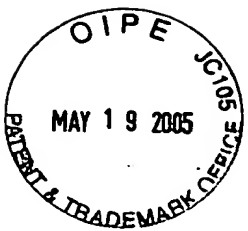
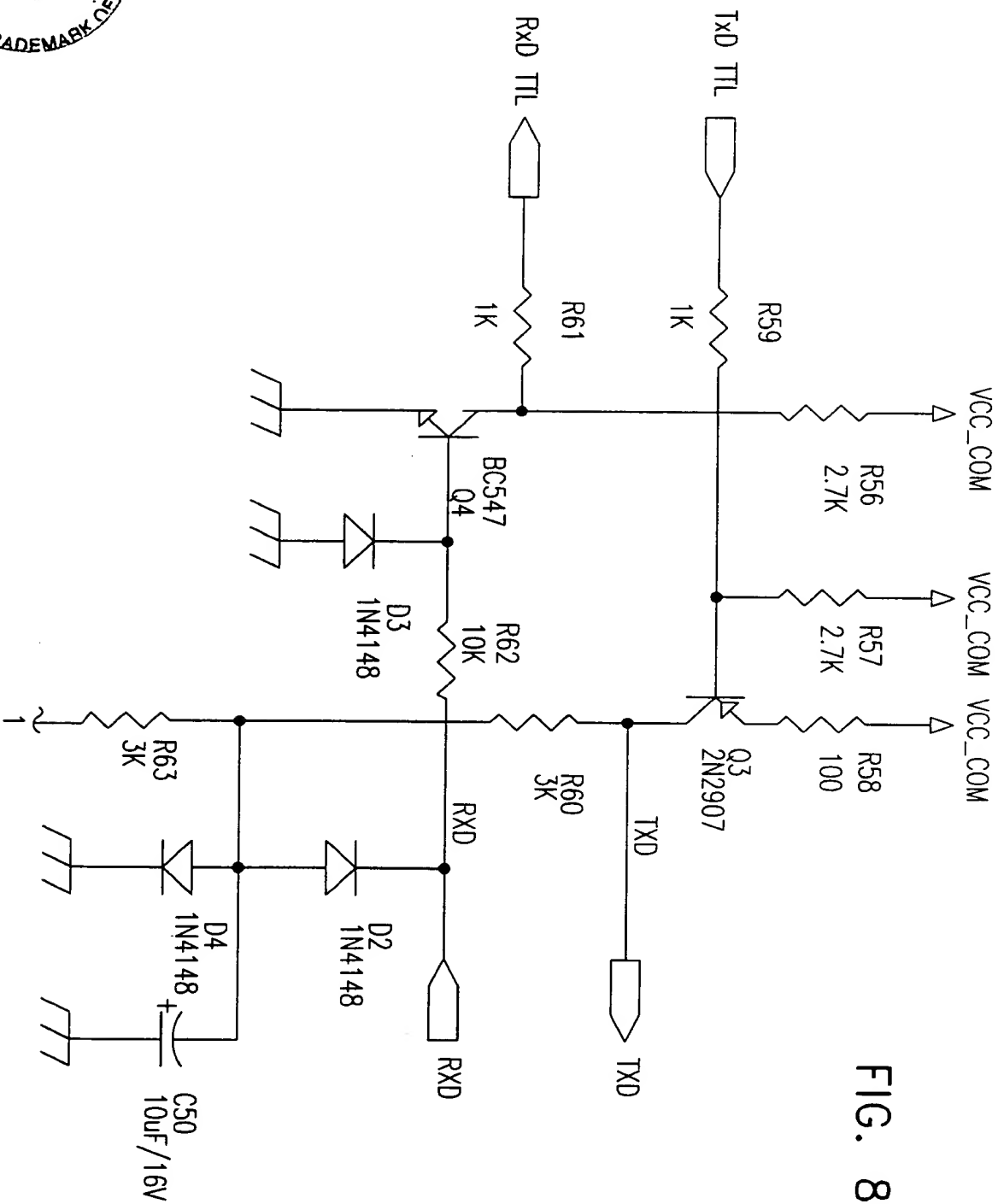


FIG. 9A/1

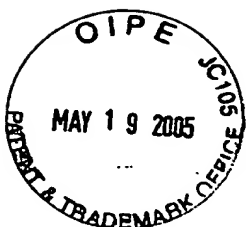
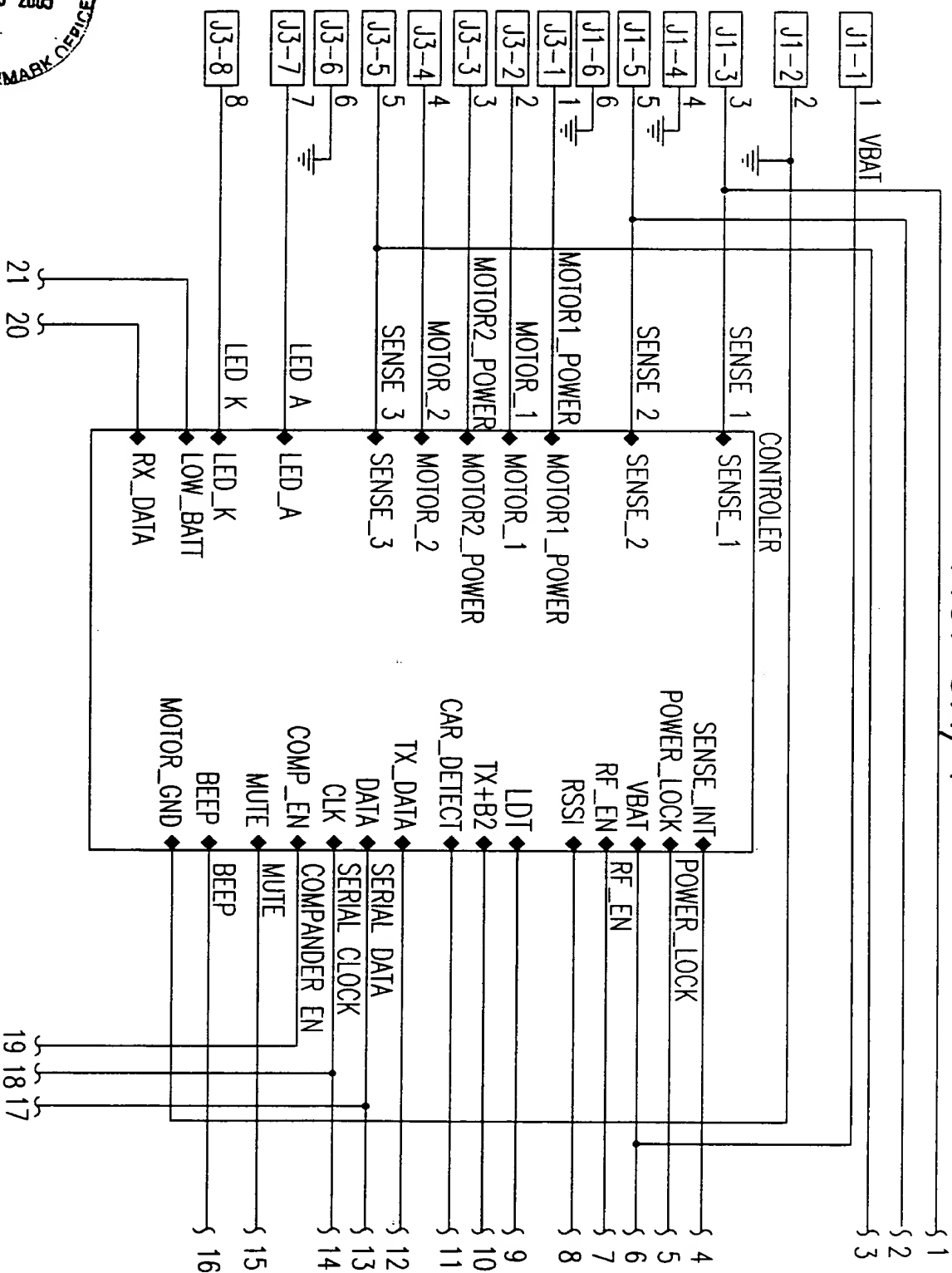


FIG. 9A/2

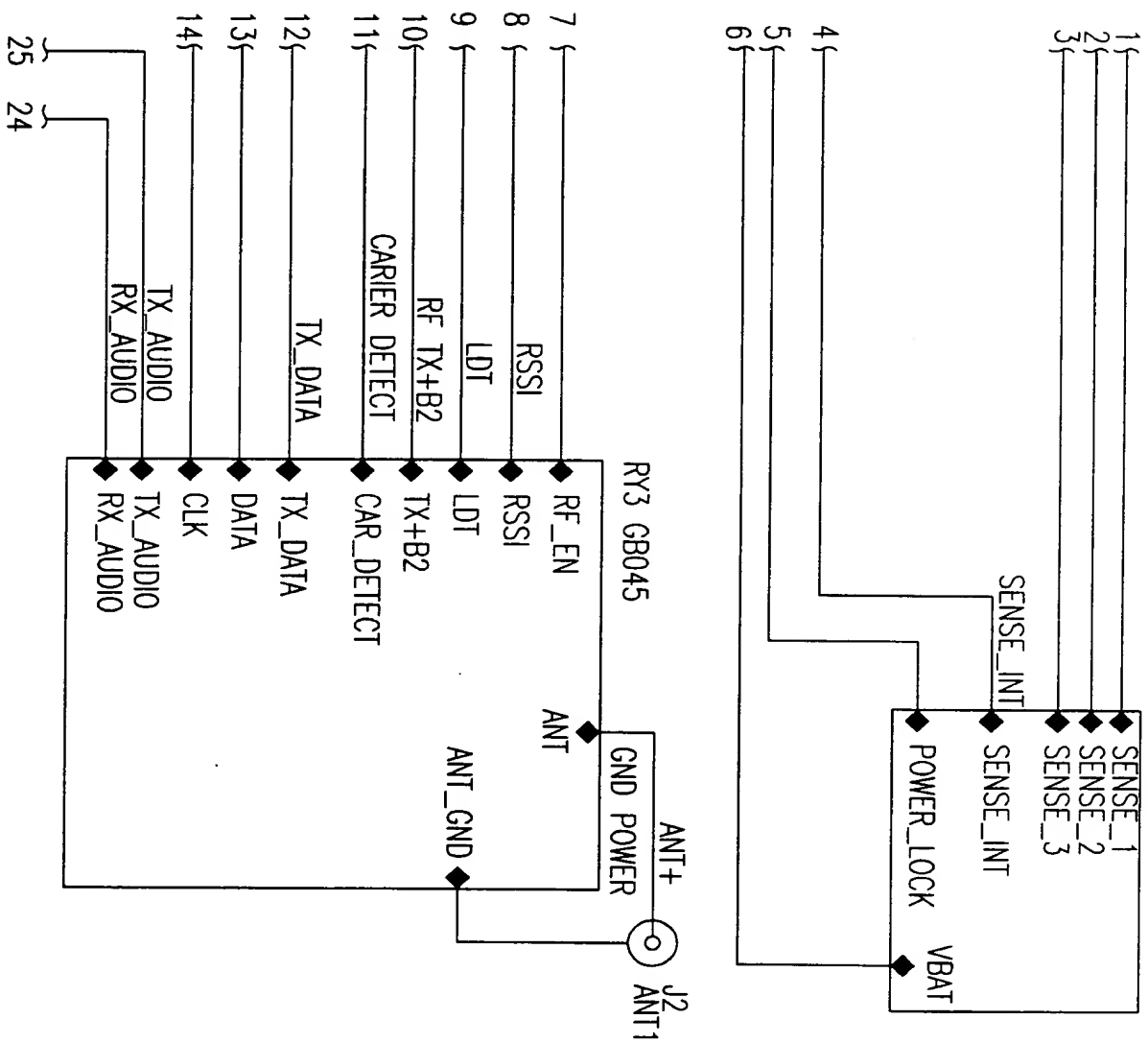


FIG. 9A/3

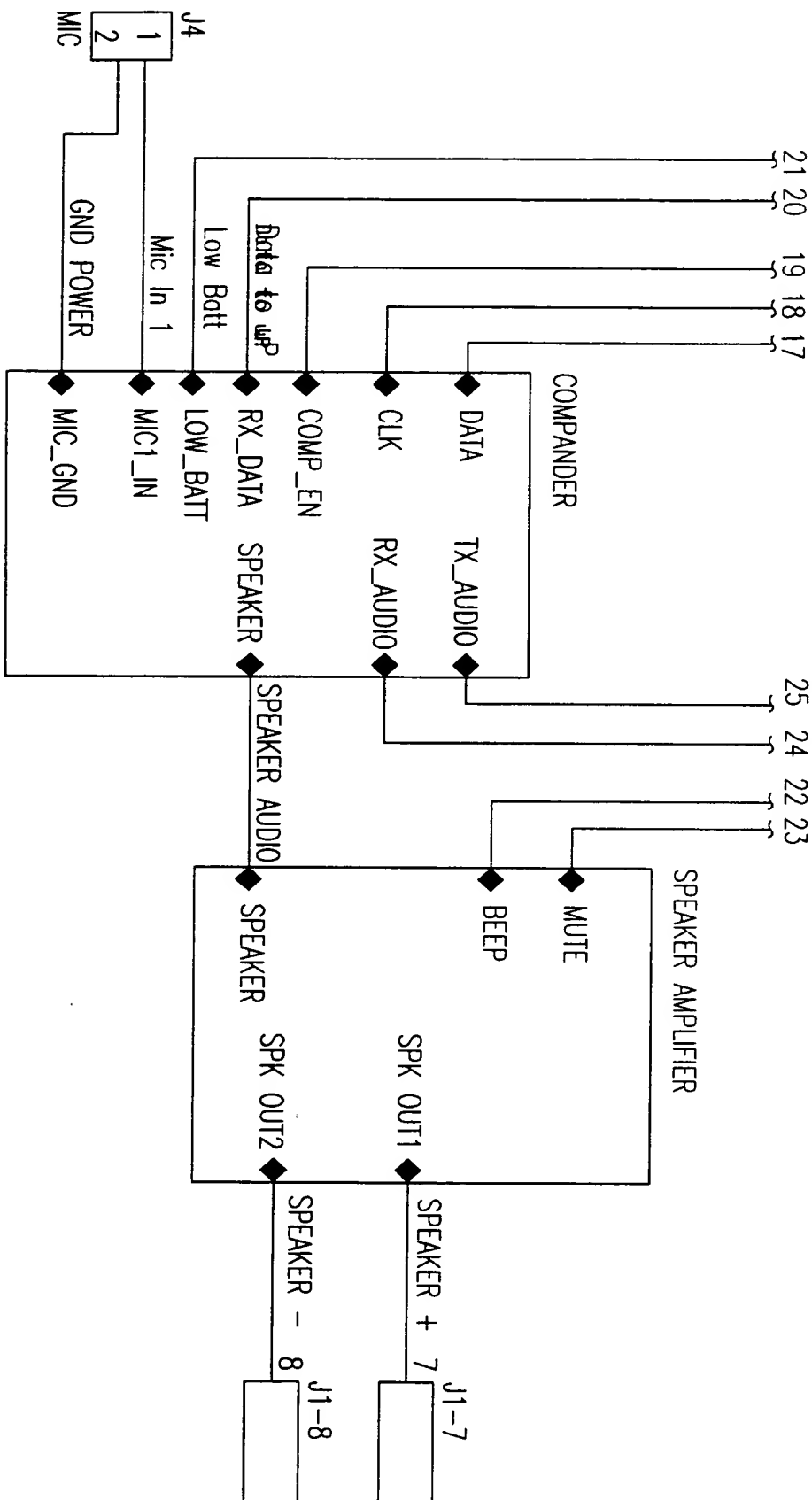


FIG. 9B/1

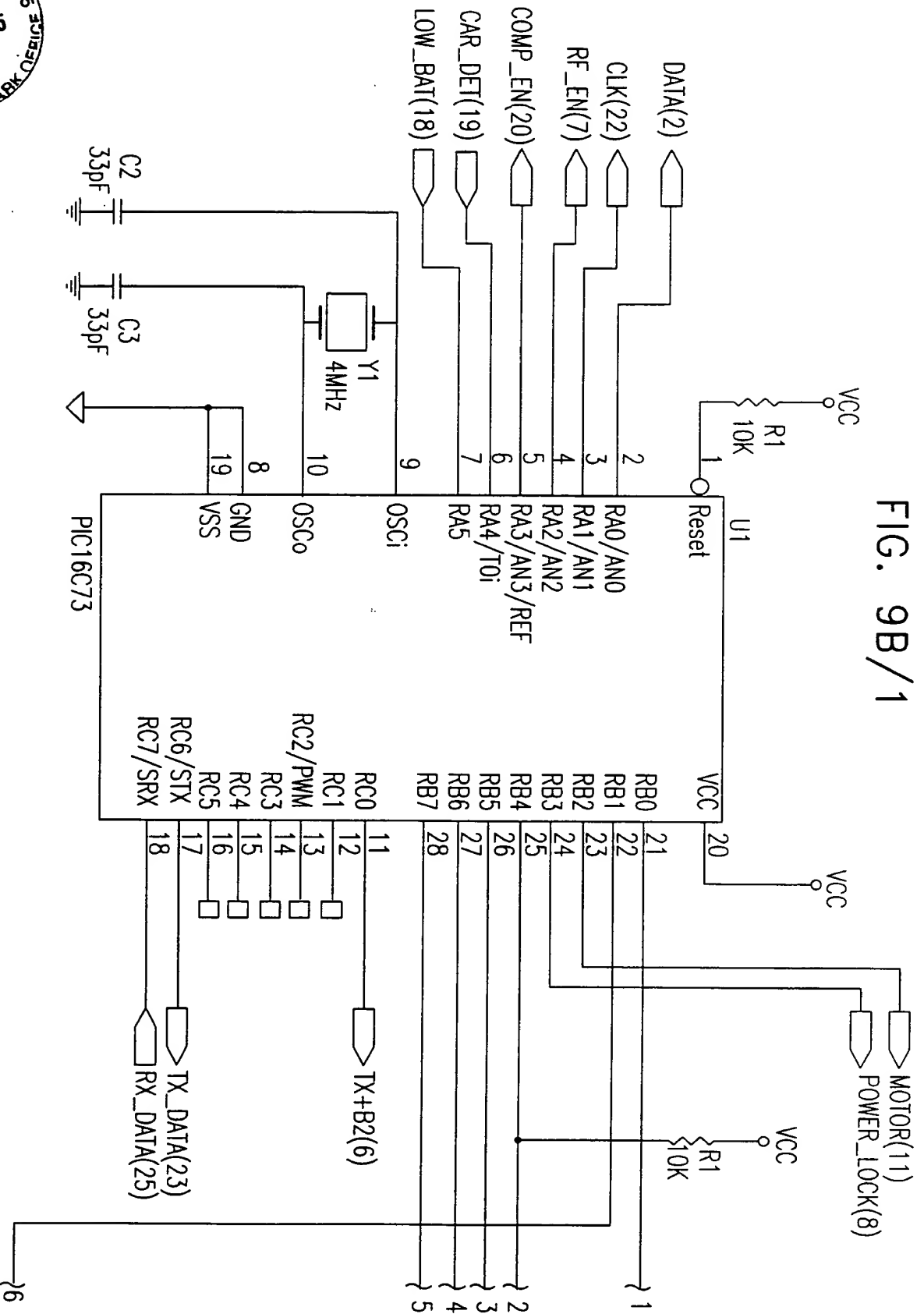


FIG. 9B/2

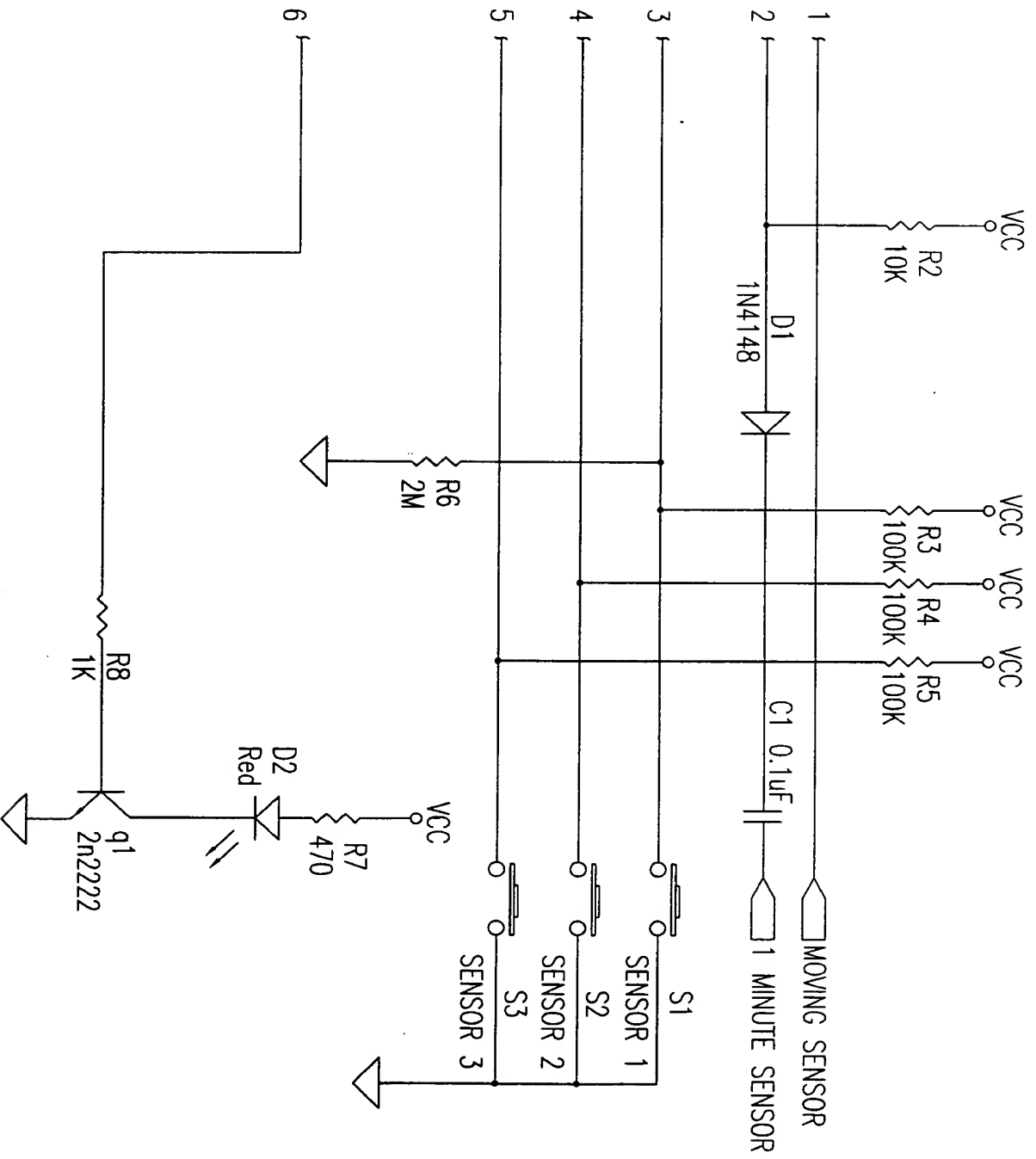
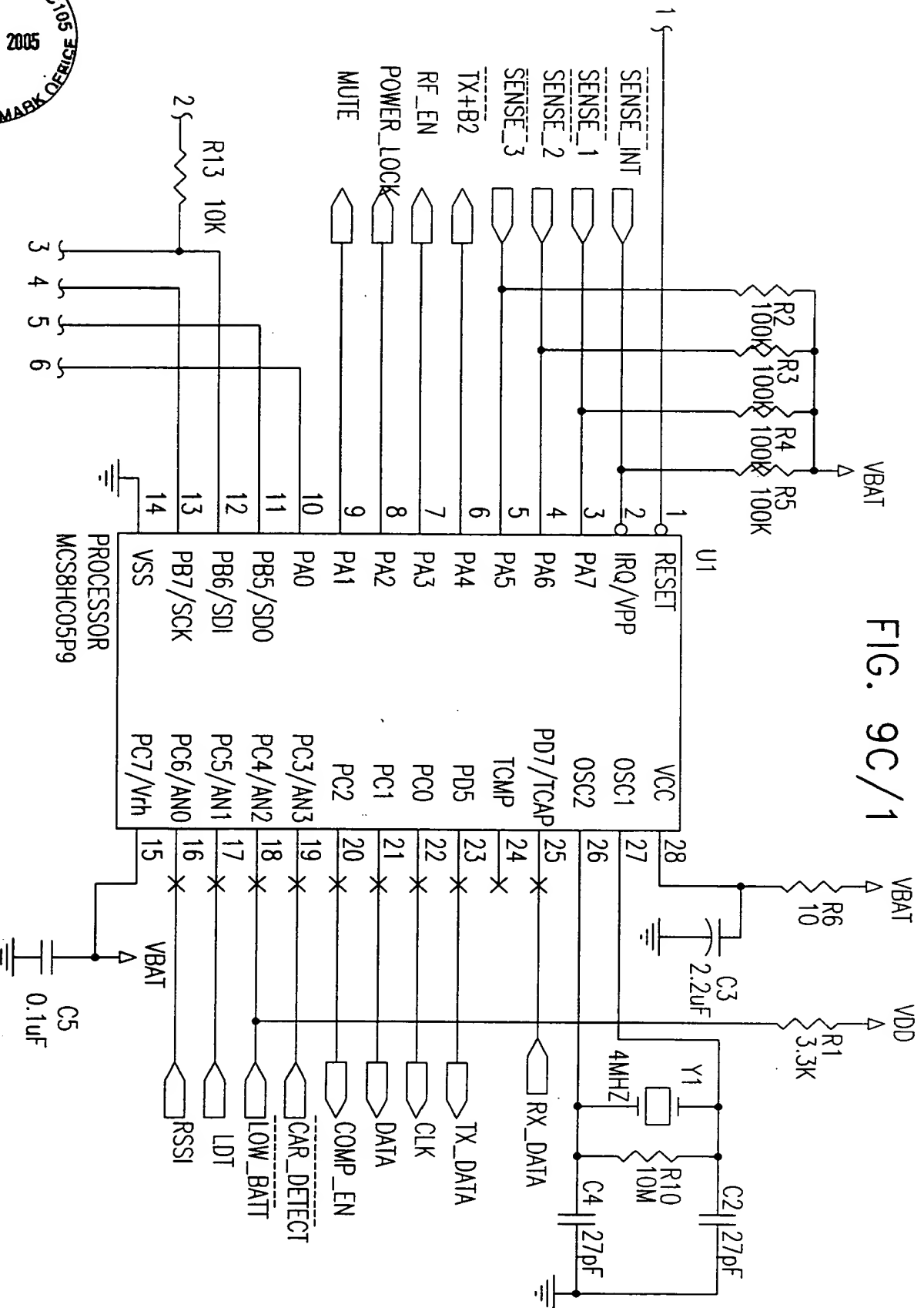


FIG. 9C/1



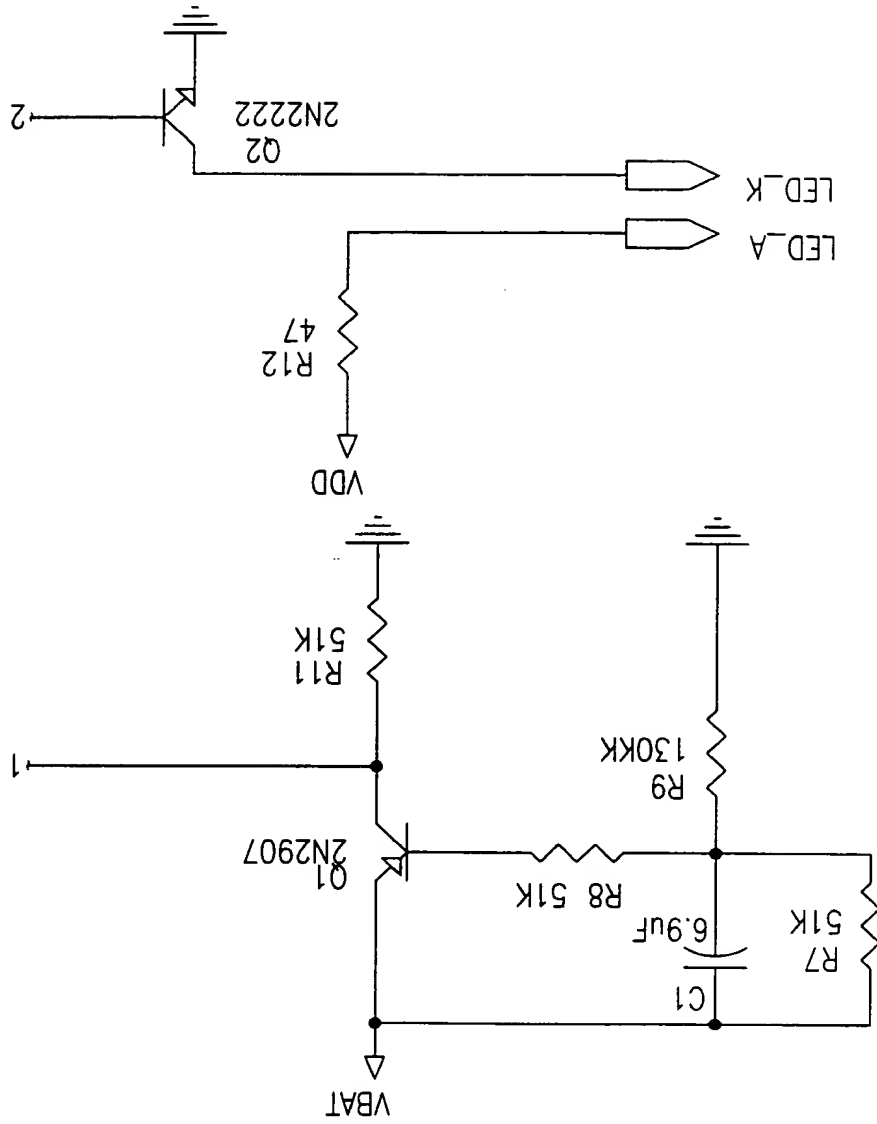
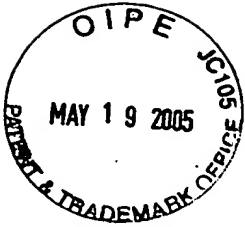


FIG. 9C/2

FIG. 9C/3

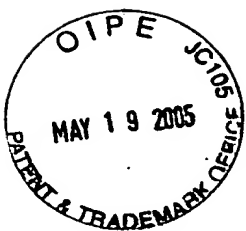
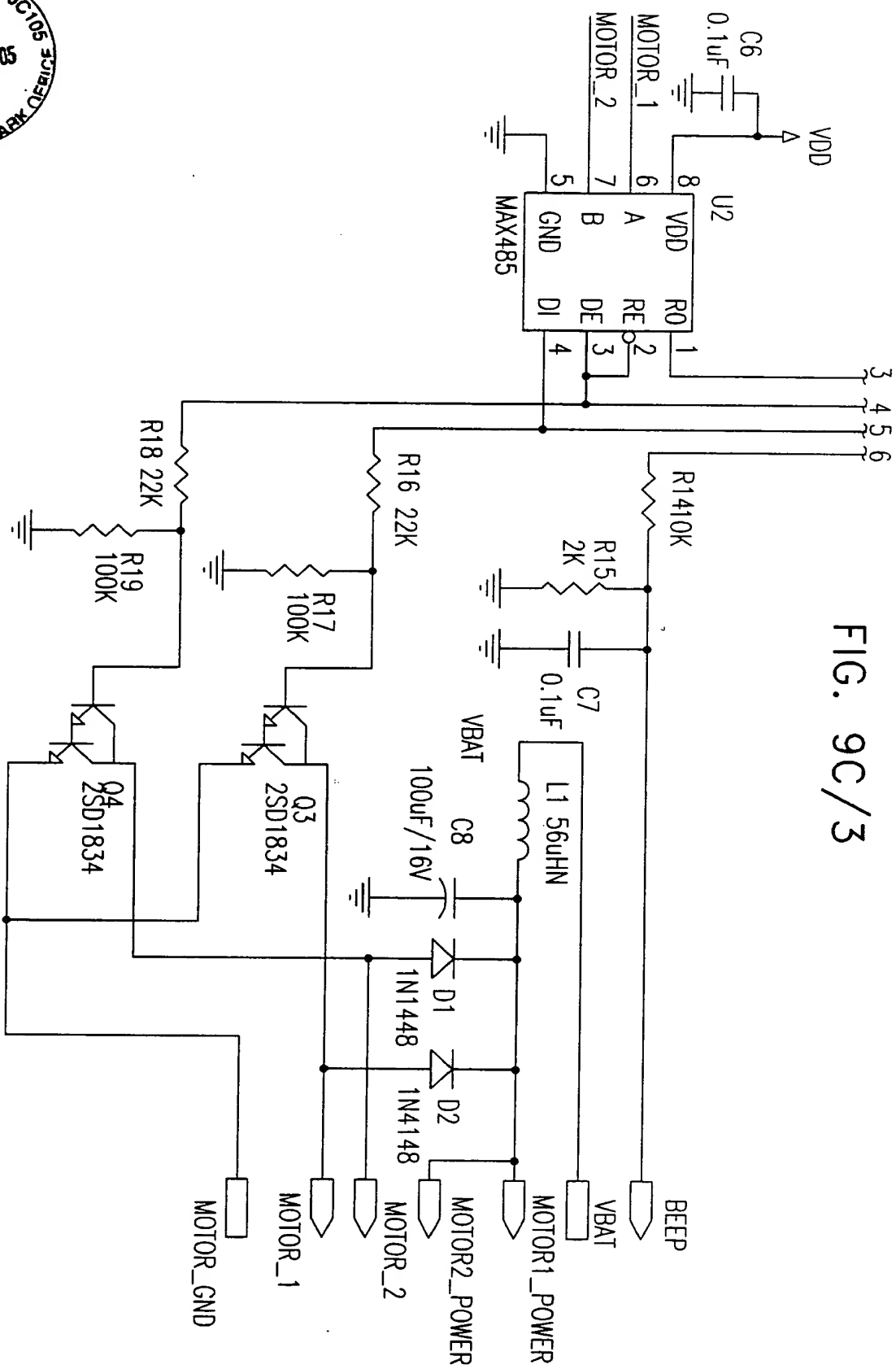
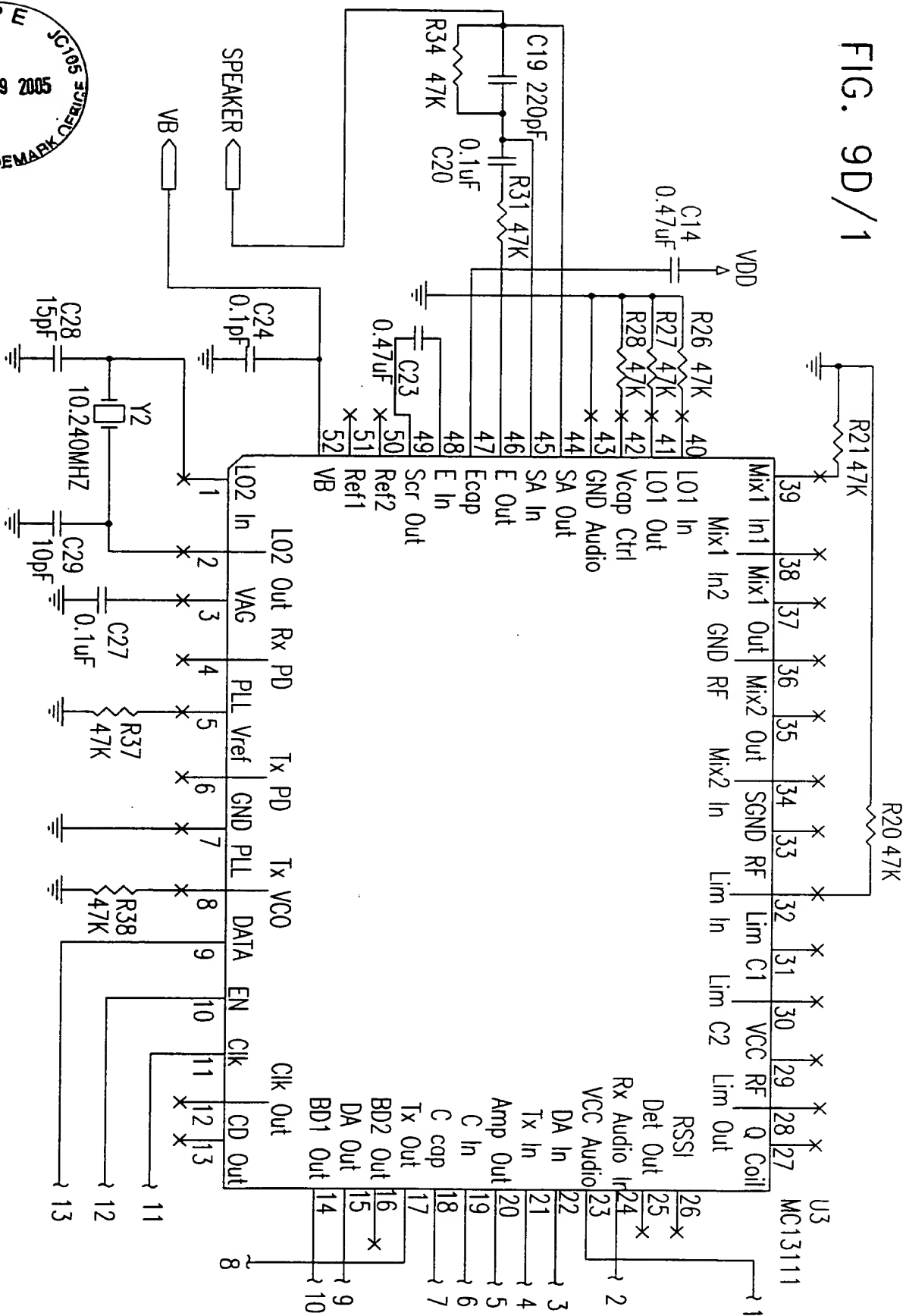
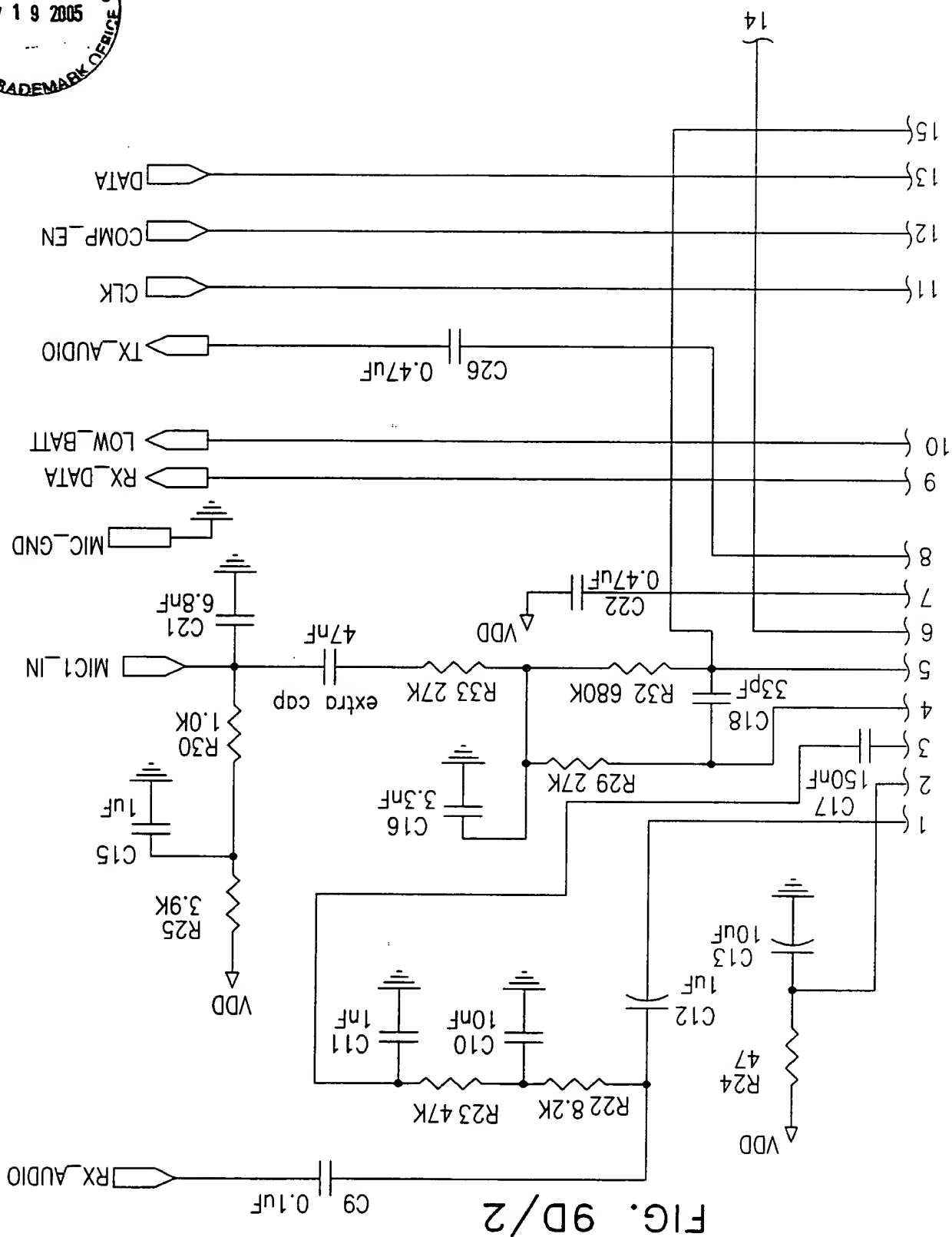


FIG. 9D/1





09/602,892

FIG. 9D/3

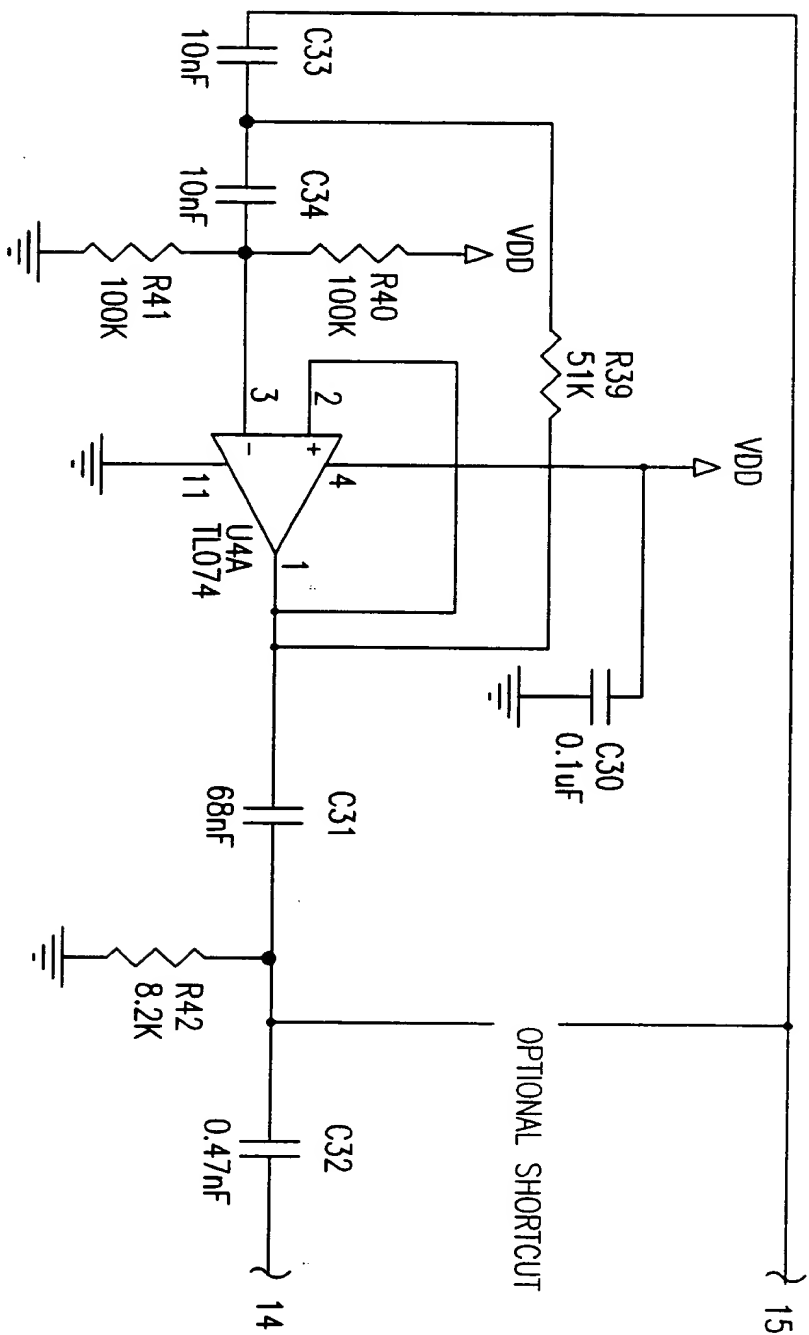


FIG. 9E/1

The circuit diagram, labeled FIG. 9E/1, illustrates a power management system. It features a VBAT input terminal connected to a VBAT node. This node is linked to a VDD node through a transistor Q5 (2N2907) and a resistor R43 (100K). A second transistor Q6 (2N2222) is connected between the VBAT node and the VDD node, with its base controlled by a POWER_LOCK signal. A resistor R44 (470) is placed between the VBAT node and the VDD node. A resistor R45 (10K) is connected between the VBAT node and a ground symbol. A resistor R46 (10K) is connected between the VBAT node and the base of Q6. The VDD node is connected to a VCC RF terminal through a coil L2 (56uHN) and a capacitor C38 (10uF). A capacitor C35 (10uF) is connected between the VCC RF terminal and ground. Additionally, capacitors C36 (10uF) and C37 (10nF) are connected between the VBAT node and ground.

FIG. 9E/2

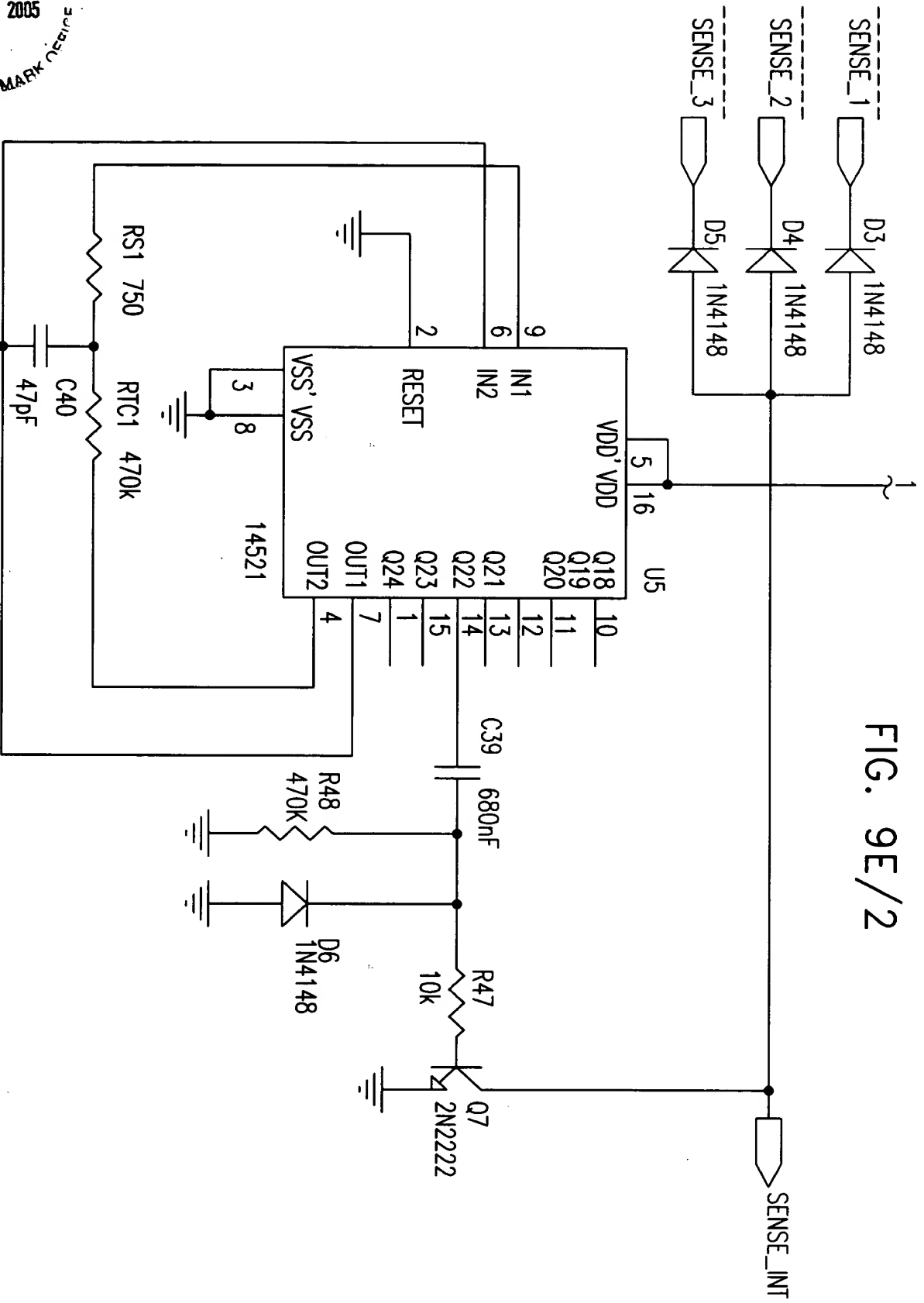


FIG. 9F

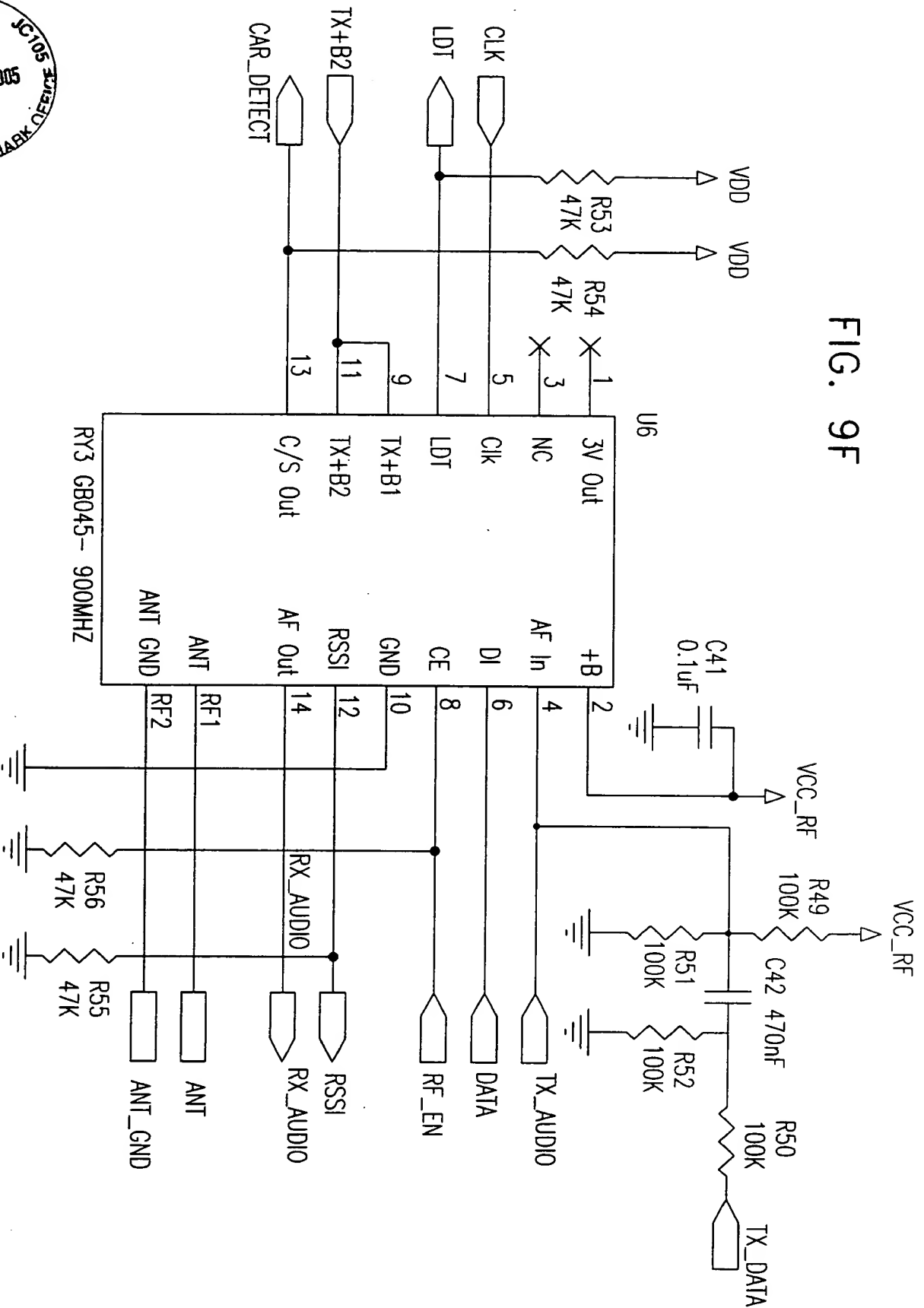


FIG. 9C

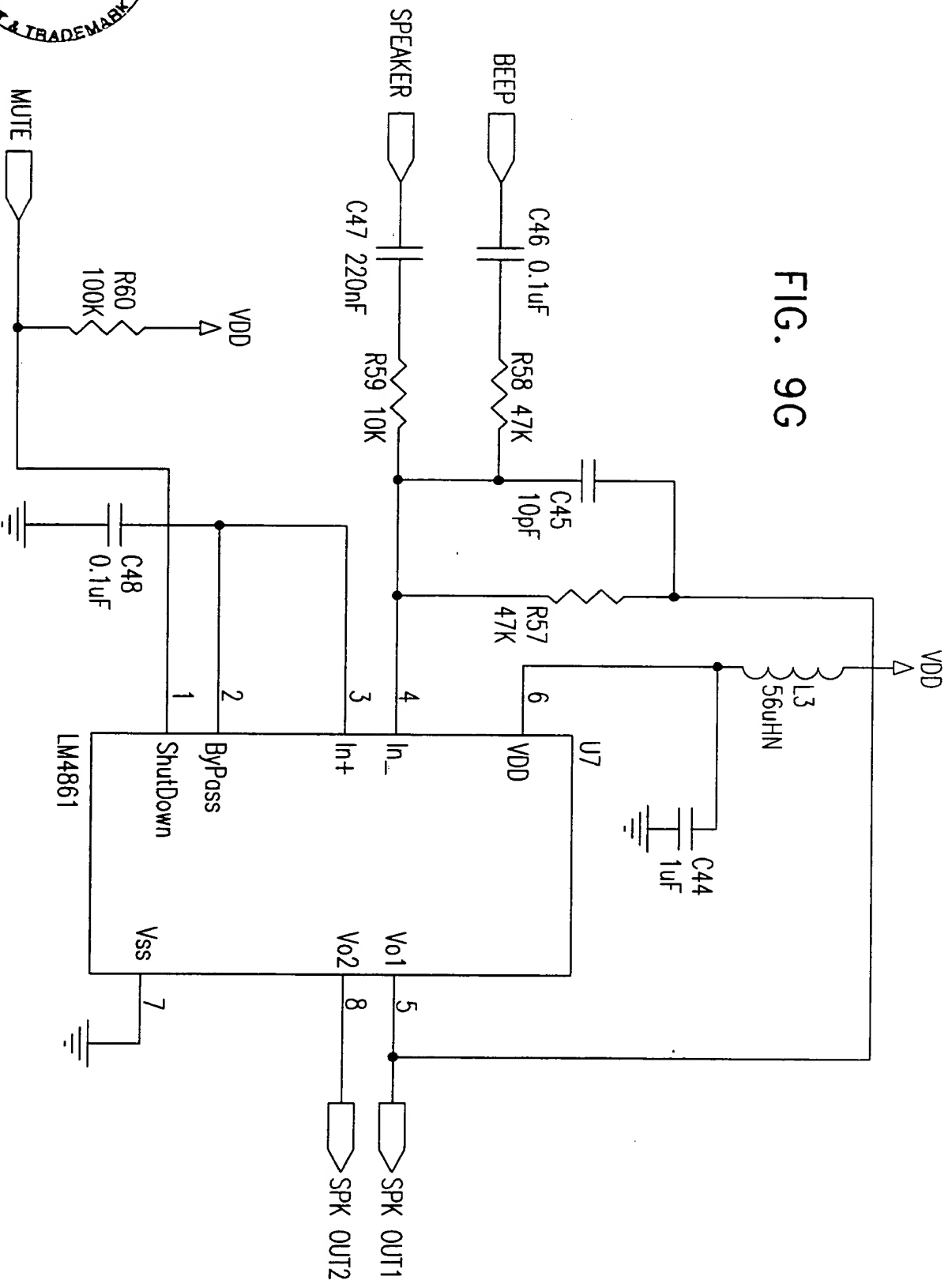


FIG. 9H/1

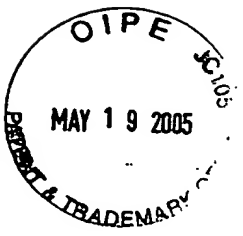
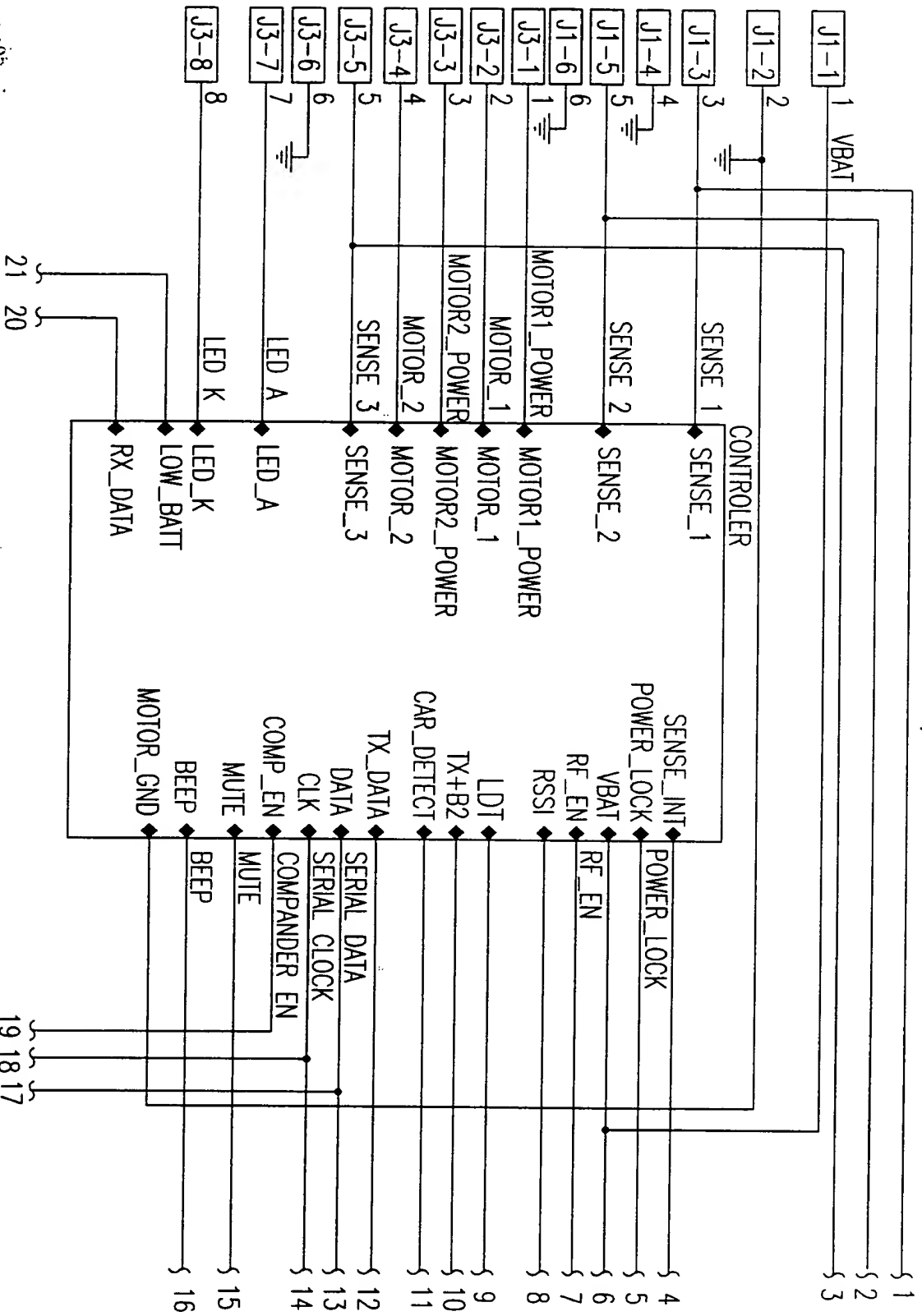


FIG. 9H/2

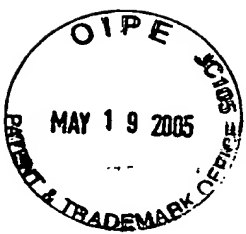
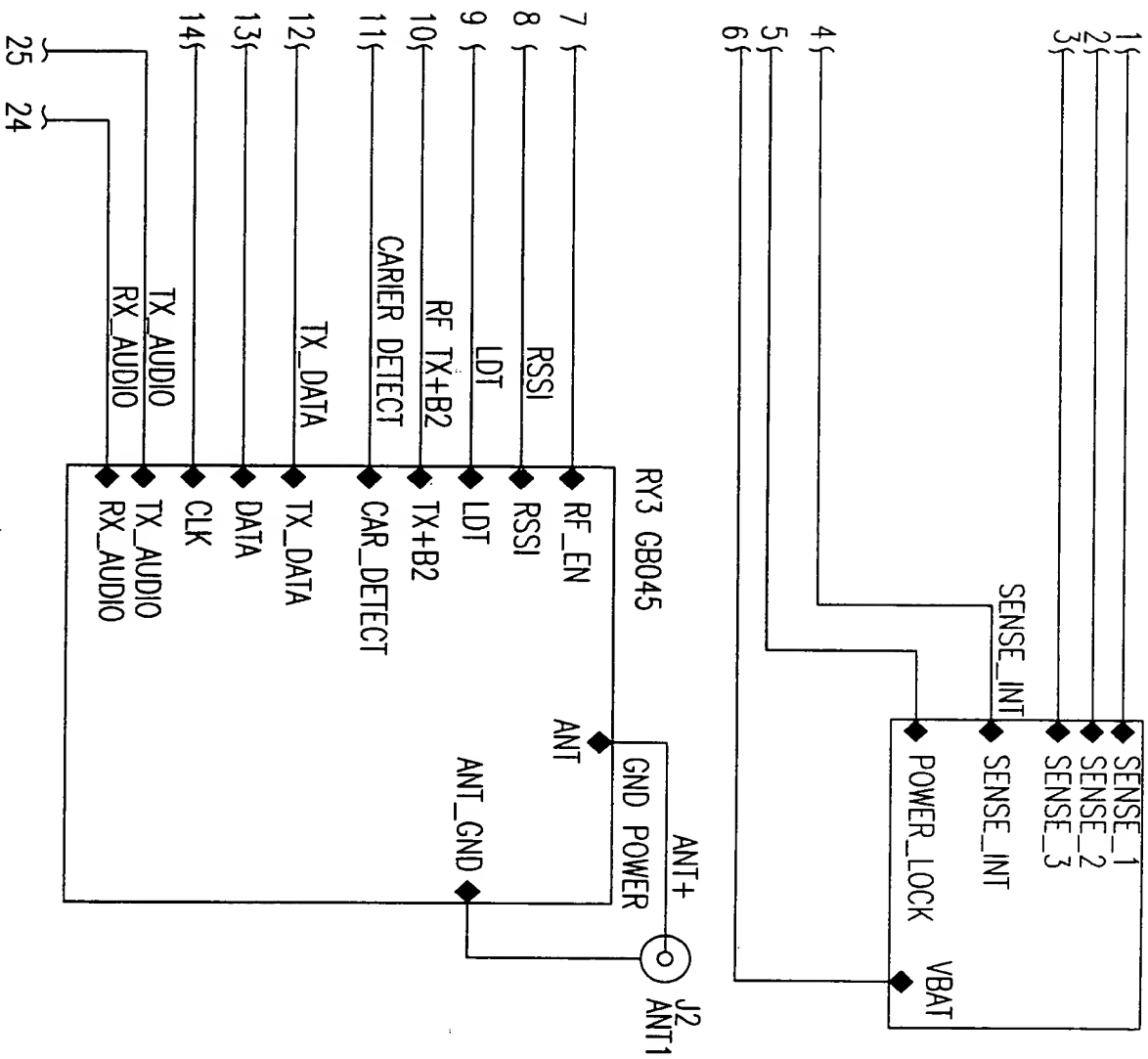


FIG. 9H/3

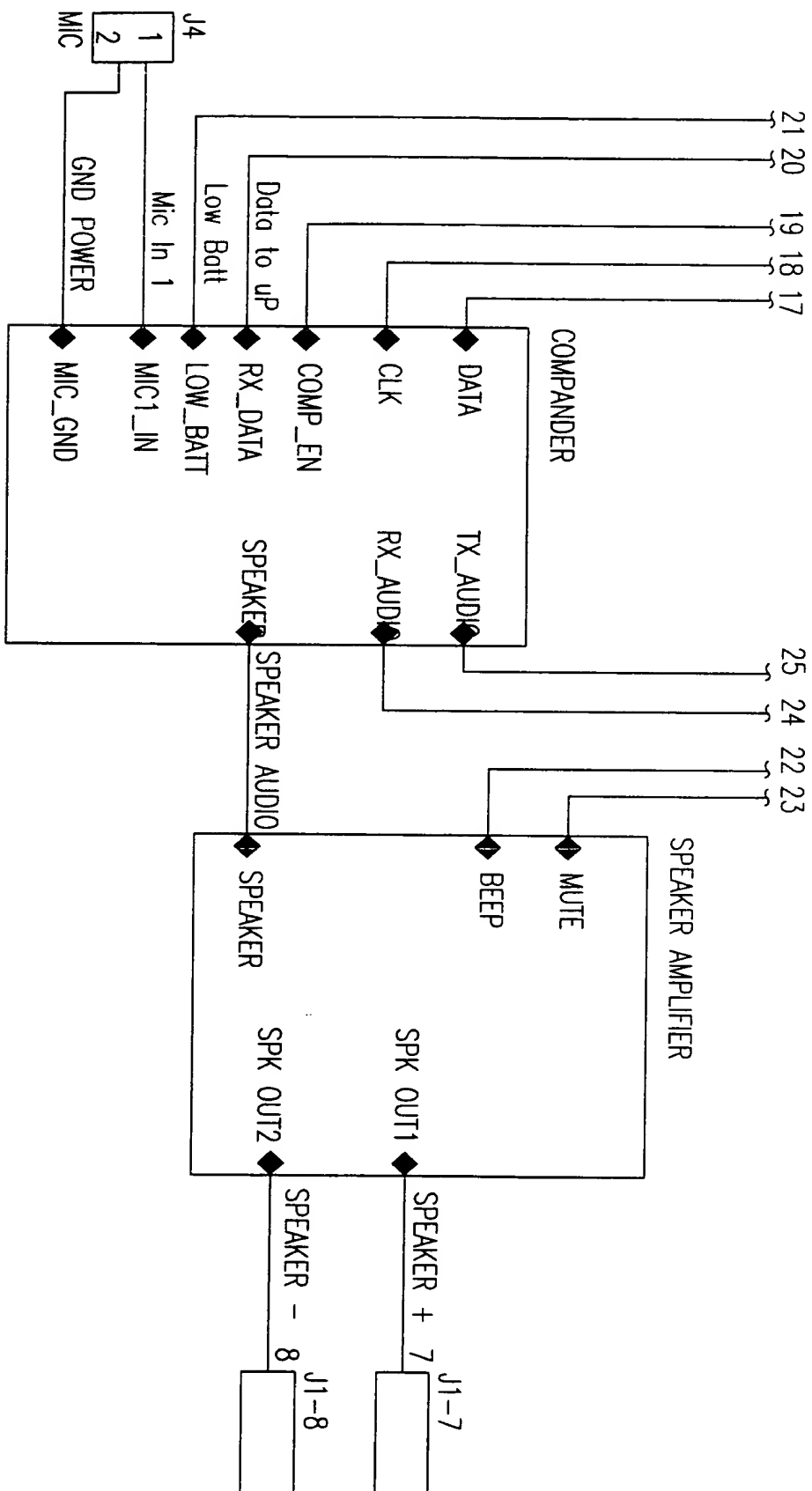
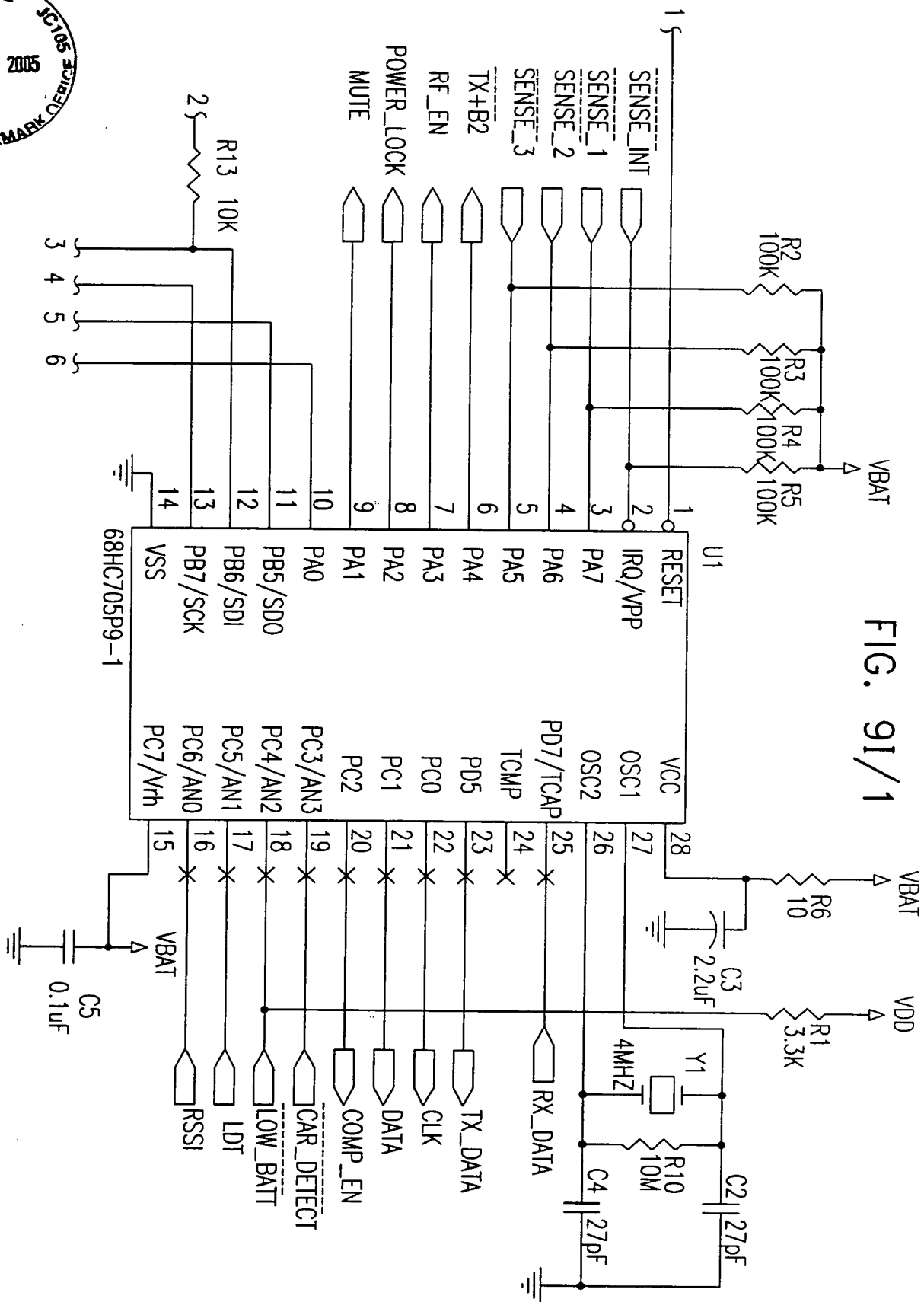


FIG. 91/1



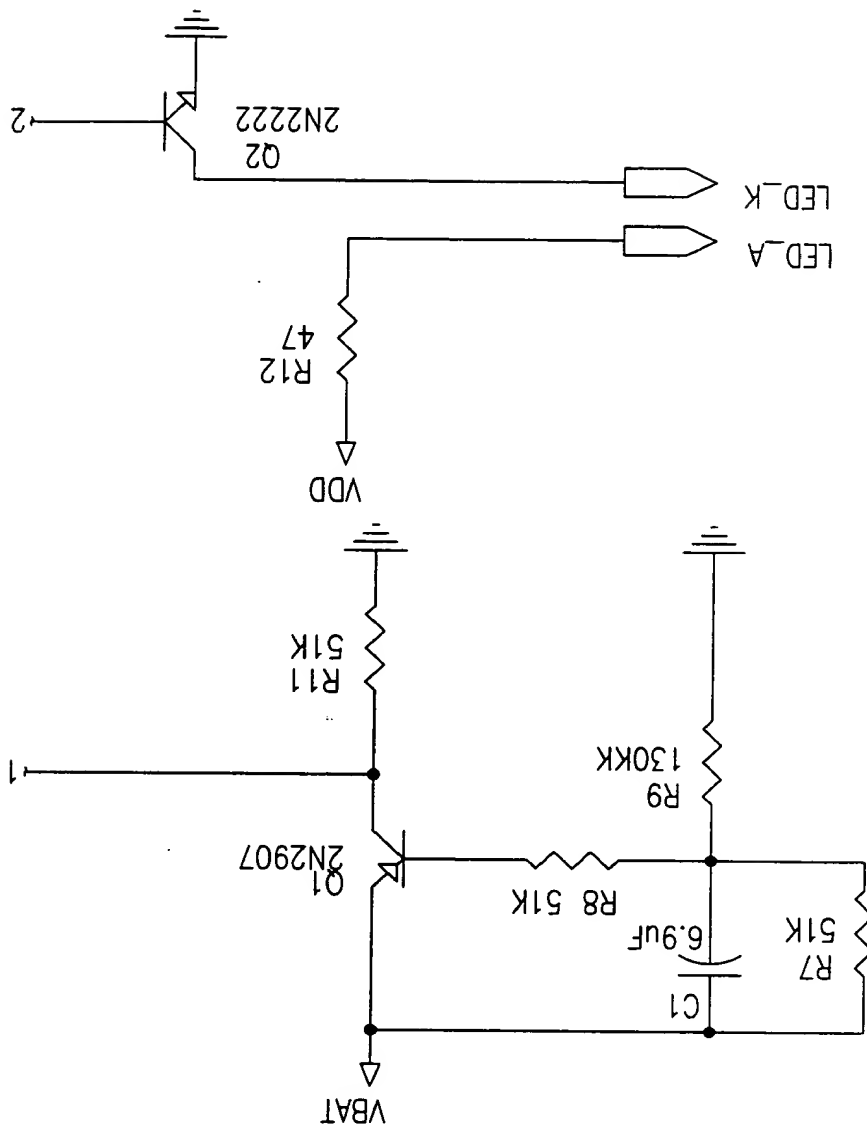


FIG. 91/2

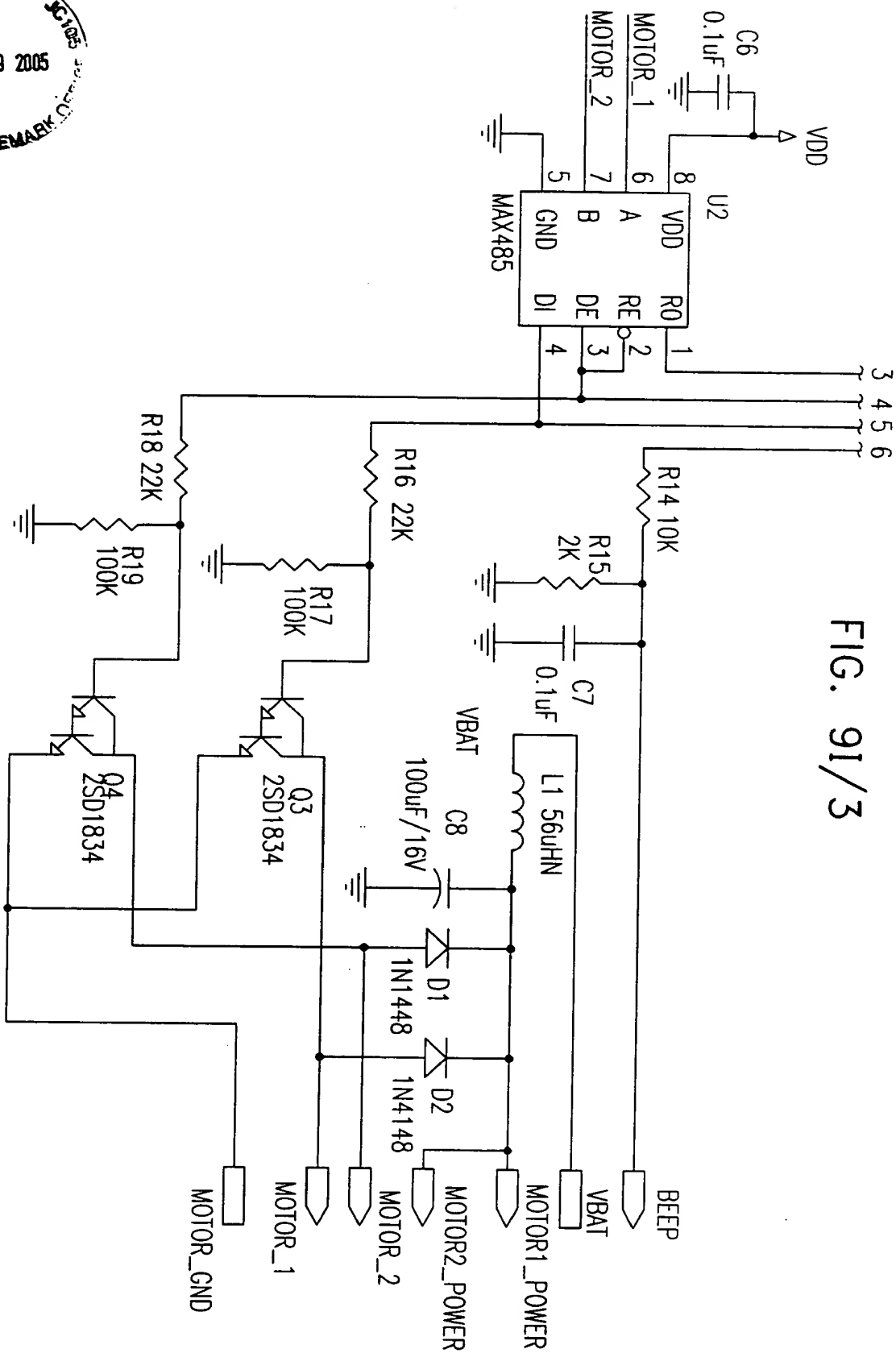
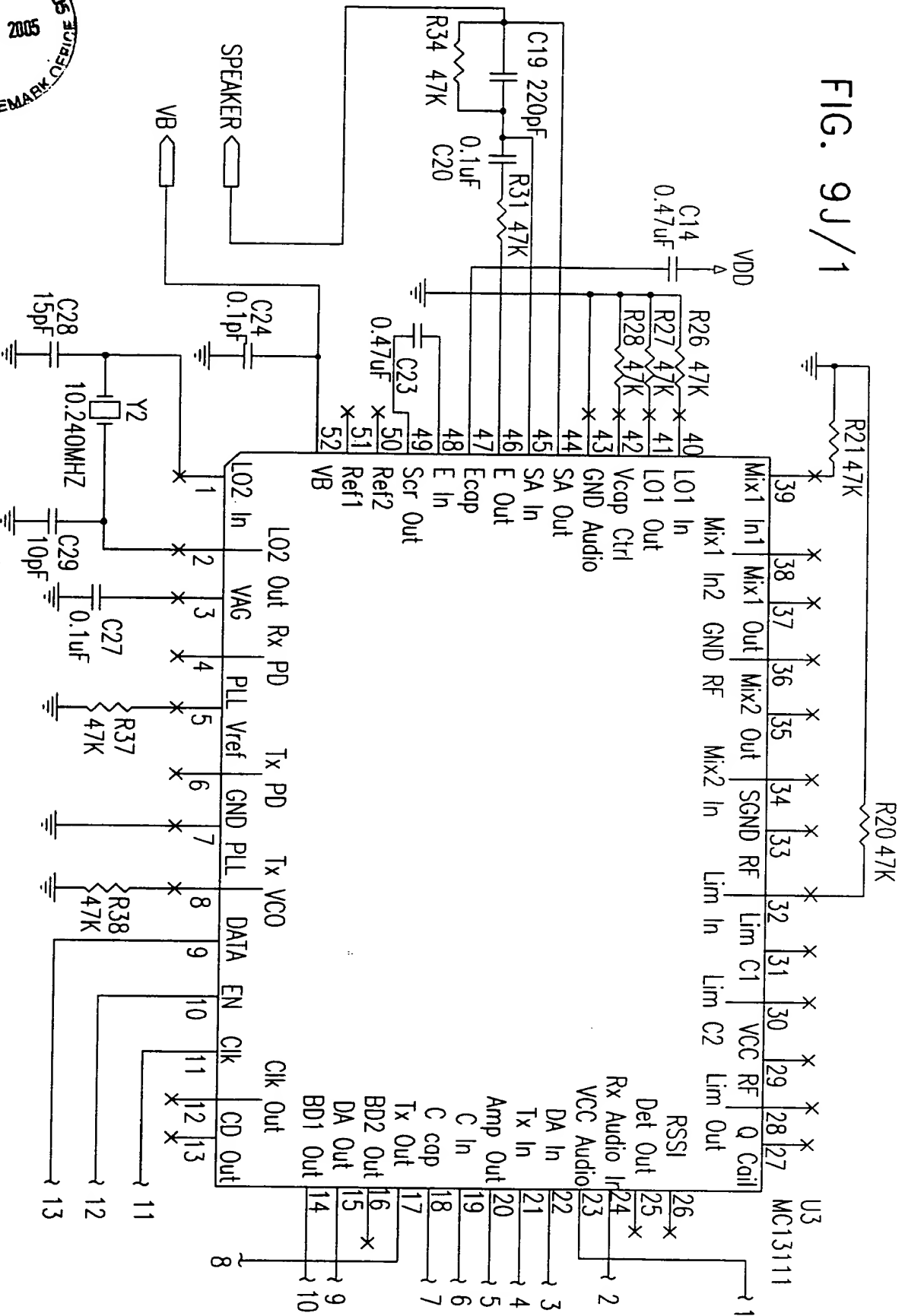


FIG. 9J/1



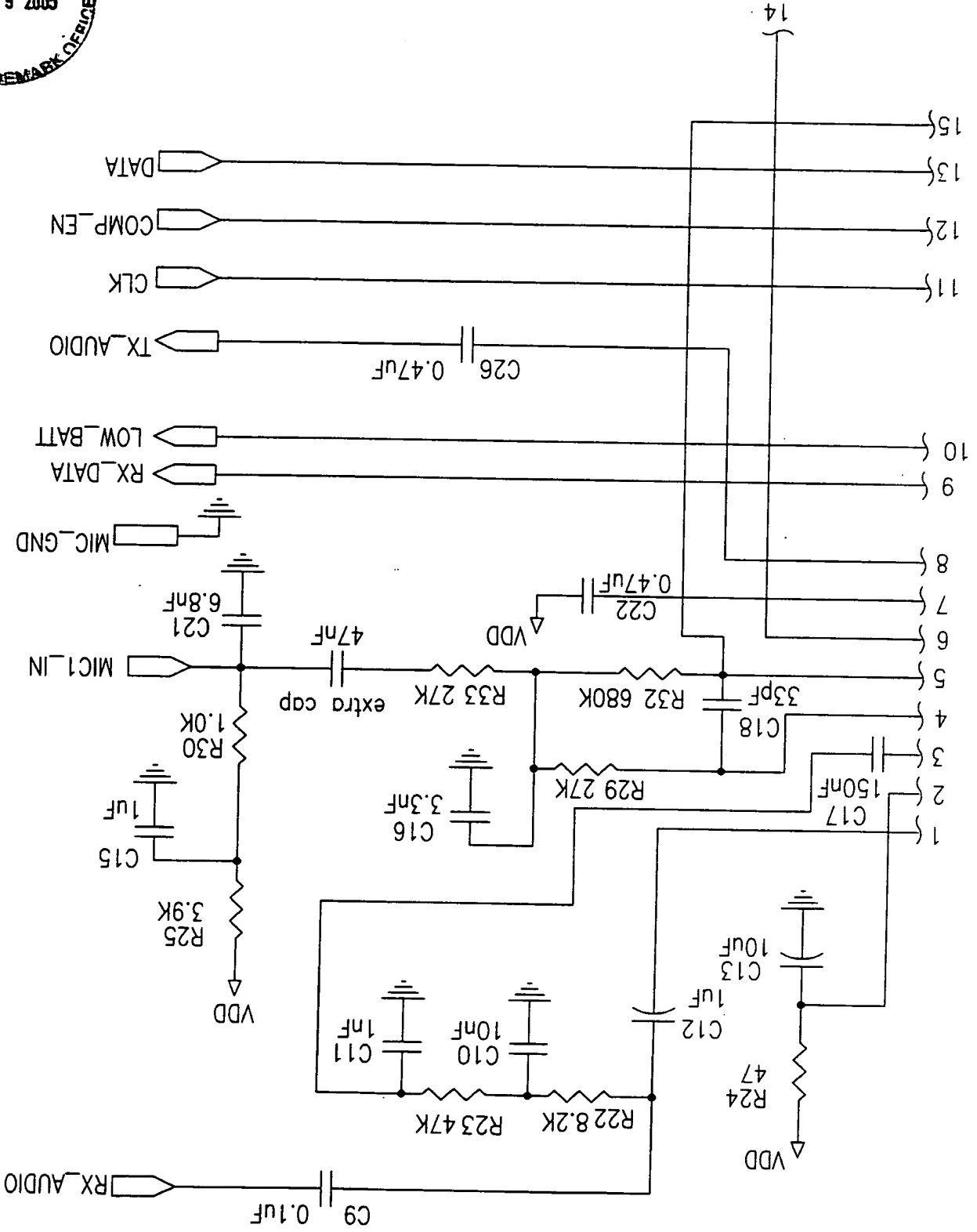
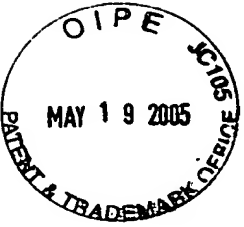


FIG. 9J/2

09/602,892

FIG. 9J/3

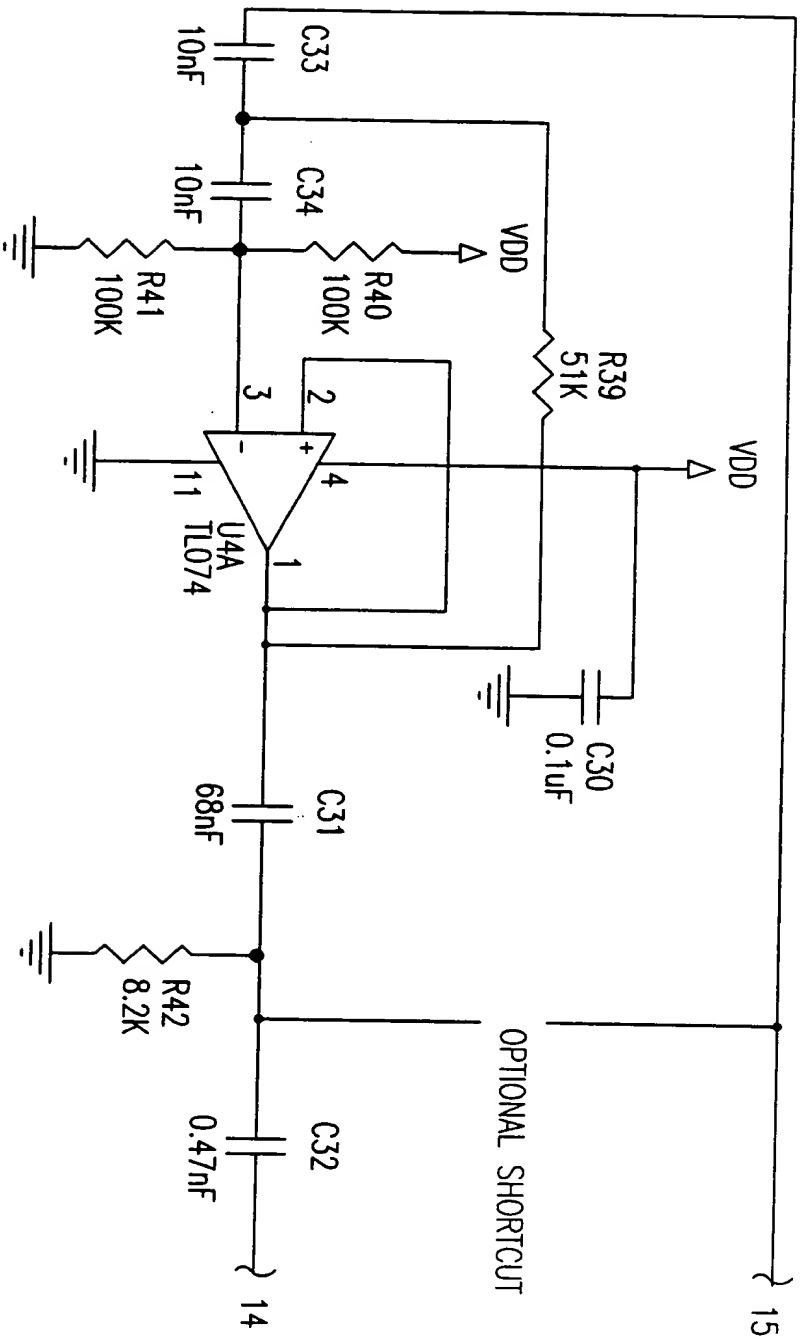


FIG. 9K/1

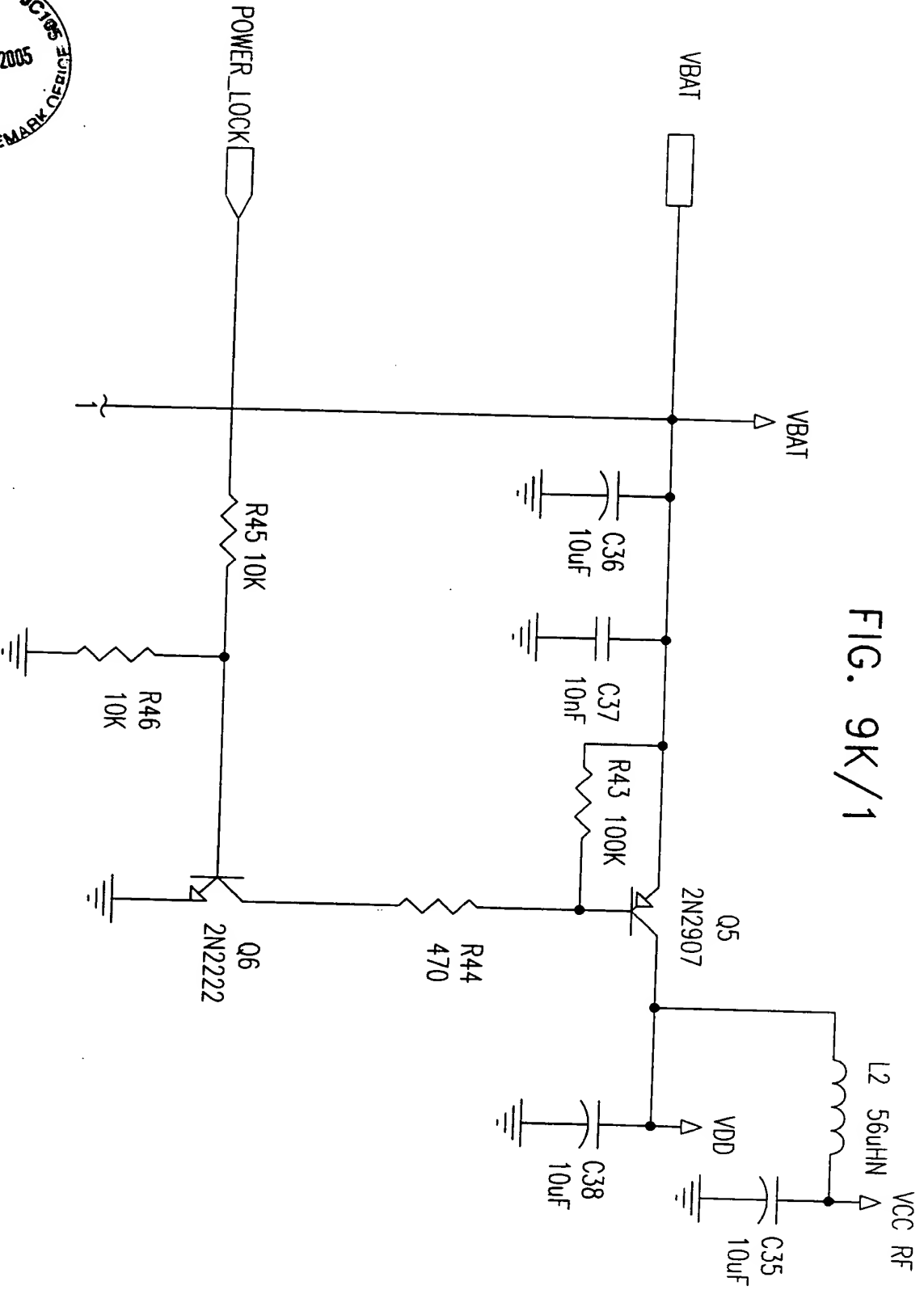


FIG. 9K/2

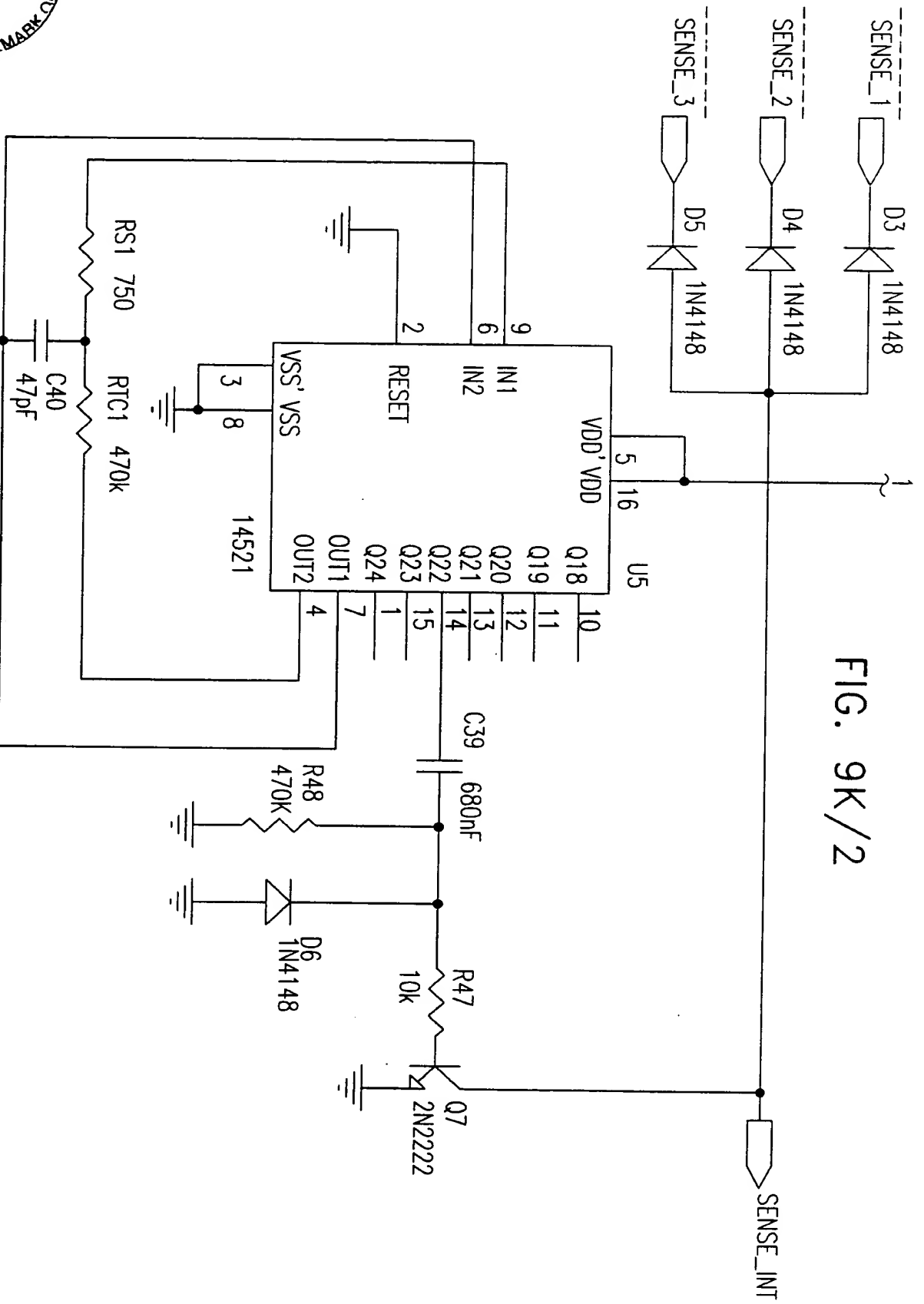


FIG. 9L

FIG. 9M

